

Compal Confidential

A4WAS MB Schematic Document

LA-C611P

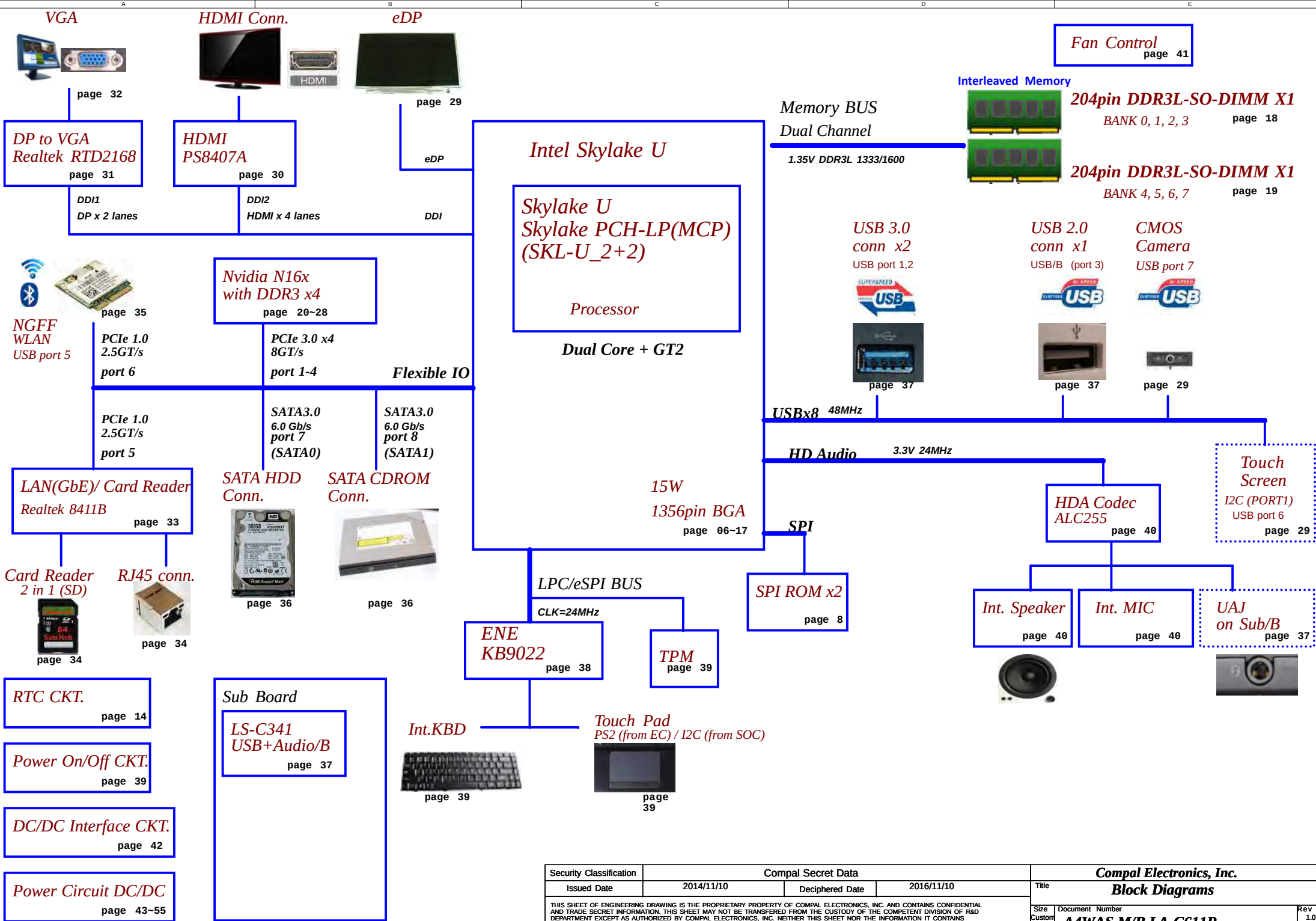
Rev: 1.0

2015.07.17

DAX

Part Number	Description
DAZ1DR00100 A4WAS_PCB_REV10	PCB A4WAS LA-C611P LS-C341P

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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				Block Diagrams	
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{BID} min	V _{BID} typ	V _{BID} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

BOM Structure Table

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	dGPU	VGA@
Connector	CONN@	N16S-GT	SGT@
EMC requirement	EMC@	N16V-GM SKU	VGM@
EMC requirement depop	@EMC@	GPU CG6 / Non GC6	NGC6@ / GC6@
CODEC(ALC255)	255@	VRAM BOM Select	X76@/X7601@ ~
CODEC(ALC283)	283@		X7614@
SPI ROM 8M*2	8M_DUAL@	Single/Dual Rank Memory Door/ No Memory Door	SR@/DR@
SPI ROM 8M*1	8M_SINGLE@		MDY@/ MDN@
UMA only	UMA@	CPU Code	PreES:QH7Y@
TPM	TPM@		ES:QHMF@, QHMG@
For Intel CMC	CMC@	No Acer IOAC	QS:QJFC@, QJ8N@, QJ8L@
For ES Sampel Only	ES@		MP:SR2EU@, SR2EY@, SR2EZ@
Keyboard backlight	KB@	CPU Code	PreES:QH7Y@
LPC MODE for EC	LPC@		ES:QHMF@, QHMG@
ESPI MODE for EC	ESPI@		QS:QJFC@, QJ8N@, QJ8L@
BA Serial	BA@	CPU Code	MP:SR2EU@, SR2EY@, SR2EZ@
EA Serial	HDD@		MP:SR2EU@, SR2EY@, SR2EZ@

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
SOC_SMBCLK +3VS	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHT(R(G-Sensor)	0x30		
SOC_SML1CLK +3VS	N16S-GT (VGA)	0x9E		
	PCH-LP (SOC)	0x90		
	BQ24780 (Charger IC)	0x12		
EC_SMB_CK1 +3VLP	BATTERY PACK	0x16		

Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

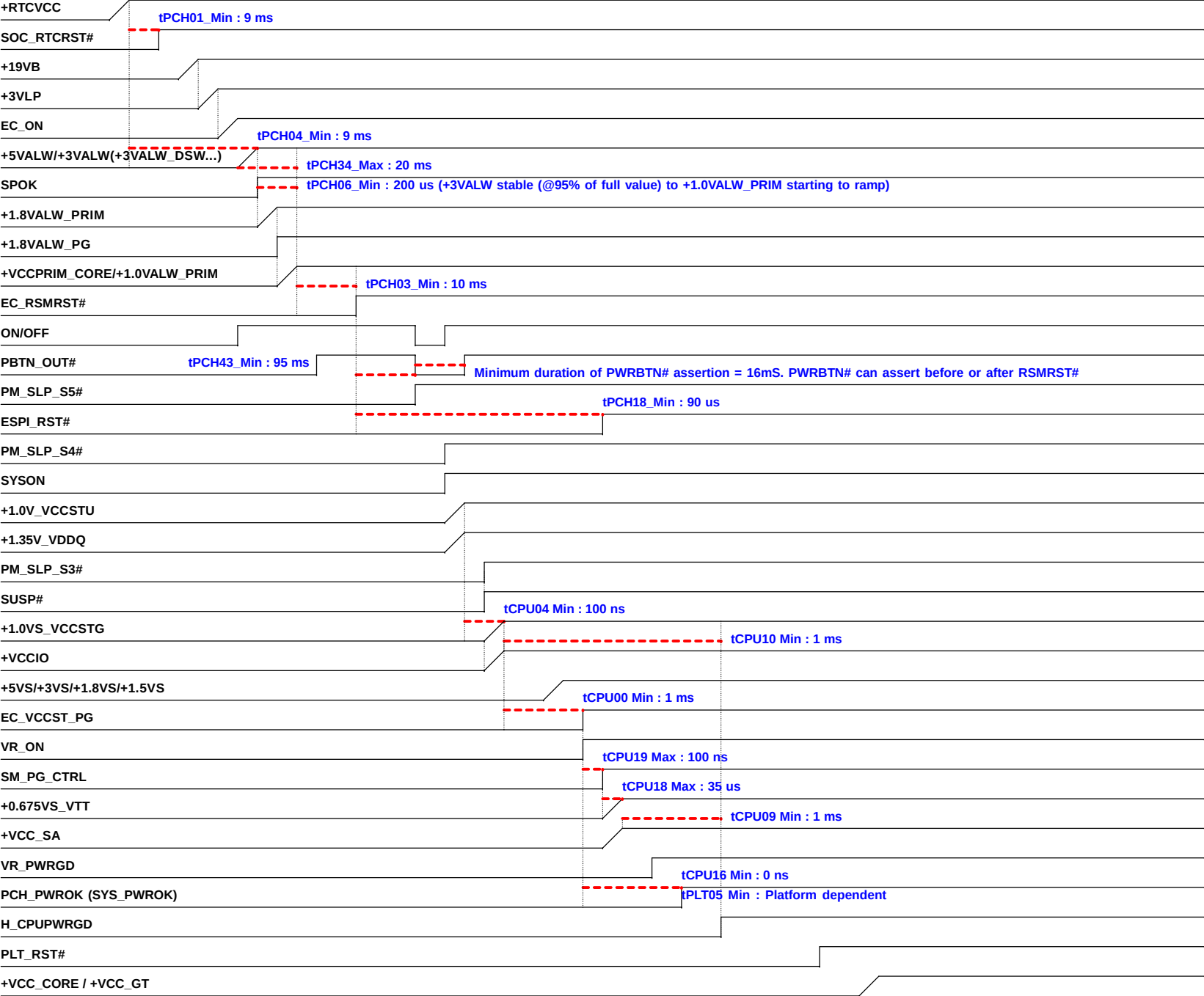
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

Voltage Rails

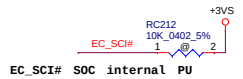
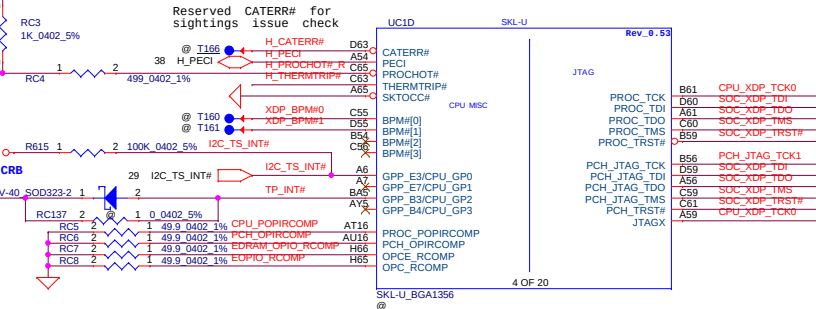
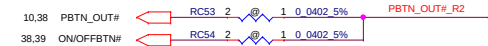
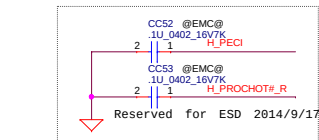
Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.675VS_VTT	DDR +0.675VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.35V_VDDQ	DDRIII.L +1.35V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON	OFF	OFF
Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.				

PWR Sequence_SKL-U2+2_DDR3L_NON CS



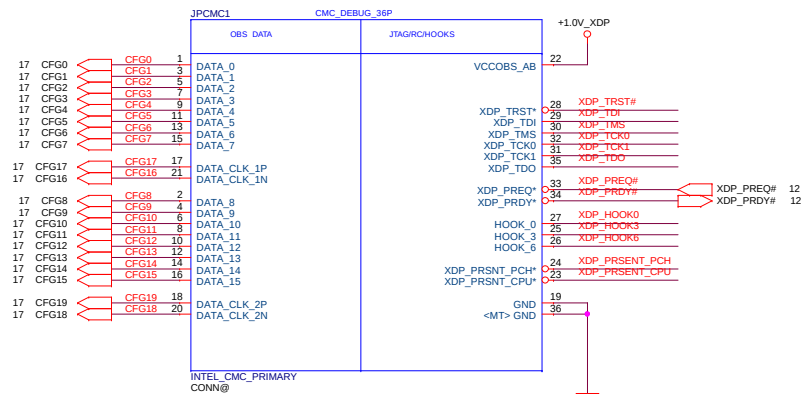
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DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port is not detected.
1 =Port is detected.



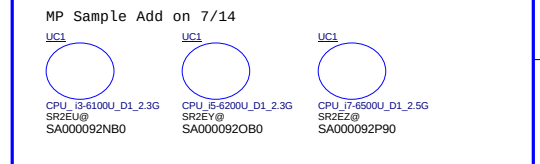
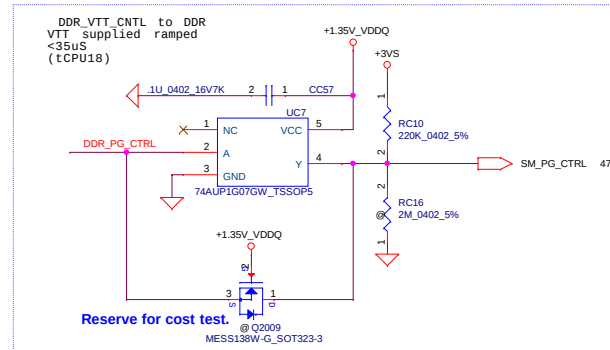
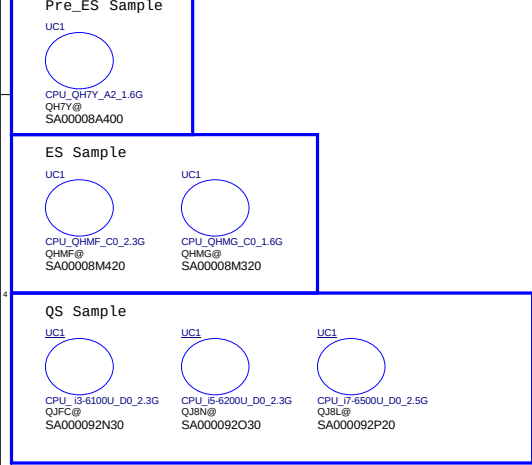
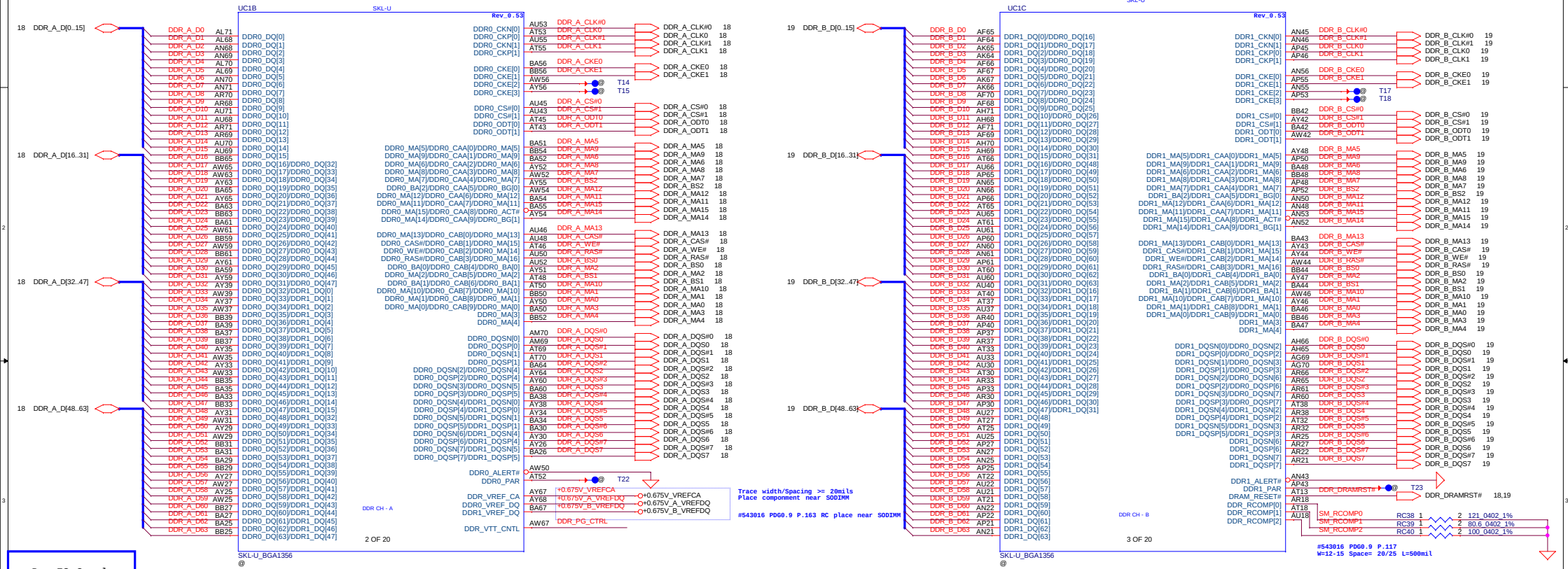
#	ATP target	Target	ATP	Device	#	ATP target	Target	ATP	Device
		QND	NA			with pre-project	with $\omega_{\text{cavity}} + \omega_{\text{probe}}$		
Notes:									
1. When light is off-resonance, the set is not an OPO/OTPA. Consider the set as a single-photon source.									
2. The OPO/OTPA is a two-photon process. The signal is $\omega_{\text{cavity}} + \omega_{\text{probe}}$.									
38	DEADCAT ₁	OTPA ₁	LO	Stokes	15	DEADCAT ₂	OTPA ₂	LO	Stokes
39	DEADCAT ₁	OTPA ₁	NA	Stokes	16	DEADCAT ₂	OTPA ₂	LO	Stokes
40	DEADCAT ₁	OTPA ₁	NA	Stokes	17	DEADCAT ₂	OTPA ₂	LO	Stokes
41	DEADCAT ₁	OTPA ₁	NA	Stokes	18	DEADCAT ₂	OTPA ₂	LO	Stokes
42	DEADCAT ₁	OTPA ₁	NA	Stokes	19	DEADCAT ₂	OTPA ₂	LO	Stokes
43	DEADCAT ₁	OTPA ₁	NA	Stokes	20	DEADCAT ₂	OTPA ₂	LO	Stokes
44	DEADCAT ₁	OTPA ₁	NA	Stokes	21	DEADCAT ₂	OTPA ₂	LO	Stokes
45	DEADCAT ₁	OTPA ₁	NA	Stokes	22	DEADCAT ₂	OTPA ₂	LO	Stokes
46	DEADCAT ₁	OTPA ₁	NA	Stokes	23	DEADCAT ₂	OTPA ₂	LO	Stokes
47	DEADCAT ₁	OTPA ₁	NA	Stokes	24	DEADCAT ₂	OTPA ₂	LO	Stokes
48	DEADCAT ₁	OTPA ₁	NA	Stokes	25	DEADCAT ₂	OTPA ₂	LO	Stokes
49	DEADCAT ₁	OTPA ₁	NA	Stokes	26	DEADCAT ₂	OTPA ₂	LO	Stokes
50	DEADCAT ₁	OTPA ₁	NA	Stokes	27	DEADCAT ₂	OTPA ₂	LO	Stokes
51	DEADCAT ₁	OTPA ₁	NA	Stokes	28	DEADCAT ₂	OTPA ₂	LO	Stokes
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55	DEADCAT ₁	OTPA ₁	NA	Stokes	32	DEADCAT ₂	OTPA ₂	LO	Stokes
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58	DEADCAT ₁	OTPA ₁	NA	Stokes	35	DEADCAT ₂	OTPA ₂	LO	Stokes
59	DEADCAT ₁	OTPA ₁	NA	Stokes	36	DEADCAT ₂	OTPA ₂	LO	Stokes
60	DEADCAT ₁	OTPA ₁	NA	Stokes	37	DEADCAT ₂	OTPA ₂	LO	Stokes
61	DEADCAT ₁	OTPA ₁	NA	Stokes	38	DEADCAT ₂	OTPA ₂	LO	Stokes
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63	DEADCAT ₁	OTPA ₁	NA	Stokes	40	DEADCAT ₂	OTPA ₂	LO	Stokes
64	DEADCAT ₁	OTPA ₁	NA	Stokes	41	DEADCAT ₂	OTPA ₂	LO	Stokes
65	DEADCAT ₁	OTPA ₁	NA	Stokes	42	DEADCAT ₂	OTPA ₂	LO	Stokes
66	DEADCAT ₁	OTPA ₁	NA	Stokes	43	DEADCAT ₂	OTPA ₂	LO	Stokes
67	DEADCAT ₁	OTPA ₁	NA	Stokes	44	DEADCAT ₂	OTPA ₂	LO	Stokes
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121	DEADCAT ₁	OTPA ₁	NA	Stokes	98	DEADCAT ₂	OTPA ₂	LO	Stokes
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142	DEADCAT ₁	OTPA ₁	NA	Stokes	119	DEADCAT ₂	OTPA ₂	LO	Stokes
143	DEADCAT ₁	OTPA ₁	NA	Stokes	120	DEADCAT ₂	OTPA ₂	LO	Stokes
144	DEADCAT ₁	OTPA ₁	NA	Stokes	121	DEADCAT ₂	OTPA ₂	LO	Stokes
145	DEADCAT ₁	OTPA ₁	NA	Stokes	122	DEADCAT ₂	OTPA ₂	LO	Stokes
146	DEADCAT ₁	OTPA ₁	NA	Stokes	123	DEADCAT ₂	OTPA ₂	LO	Stokes
147	DEADCAT ₁	OTPA ₁	NA	Stokes	124	DEADCAT ₂	OTPA ₂	LO	Stokes
148	DEADCAT ₁	OTPA ₁	NA	Stokes	125	DEADCAT ₂	OTPA ₂	LO	Stokes
149	DEADCAT ₁	OTPA ₁	NA	Stokes	126	DEADCAT ₂	OTPA ₂	LO	Stokes
150	DEADCAT ₁	OTPA ₁	NA	Stokes	127	DEADCAT ₂	OTPA ₂	LO	Stokes
151	DEADCAT ₁	OTPA ₁	NA	Stokes	128	DEADCAT ₂	OTPA ₂	LO	Stokes
152	DEADCAT ₁	OTPA ₁	NA	Stokes	129	DEADCAT ₂	OTPA ₂	LO	Stokes
153	DEADCAT ₁	OTPA ₁	NA	Stokes	130	DEADCAT ₂	OTPA ₂	LO	Stokes
154	DEADCAT ₁	OTPA ₁	NA	Stokes	131	DEADCAT ₂	OTPA ₂	LO	Stokes
155	DEADCAT ₁	OTPA ₁	NA	Stokes	132	DEADCAT ₂	OTPA ₂	LO	Stokes
156	DEADCAT ₁	OTPA ₁	NA	Stokes	133	DEADCAT ₂	OTPA ₂	LO	Stokes
157	DEADCAT ₁	OTPA ₁	NA	Stokes	134	DEADCAT ₂	OTPA ₂	LO	Stokes
158	DEADCAT ₁	OTPA ₁	NA	Stokes	135	DEADCAT ₂	OTPA ₂	LO	Stokes
159	DEADCAT ₁	OTPA ₁	NA	Stokes	136	DEADCAT ₂	OTPA ₂	LO	Stokes
160	DEADCAT ₁	OTPA ₁	NA	Stokes	137	DEADCAT ₂			

```
#545659 PCH EDS 0.7 P.108
SCI capability is available on all GPIOs,
while NMI and SMI capability is available on
selected GPIOs only.
Below are the PCH GPIOs that can be routed to
generate SMI# or NMI:
  * GPP_B14,   GPP_B20,   GPP_B23
  * GPP_C[23:22]
  * GPP_D[4:0]
  * GPP_E[8:0],   GPP_E[16:13]
```

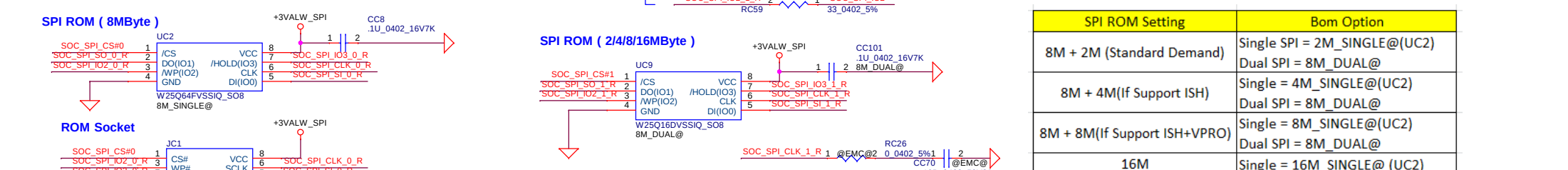
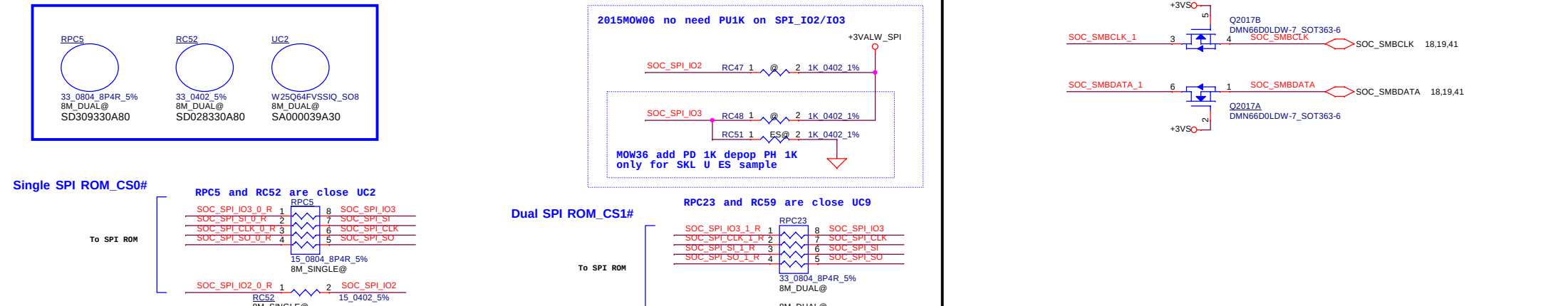
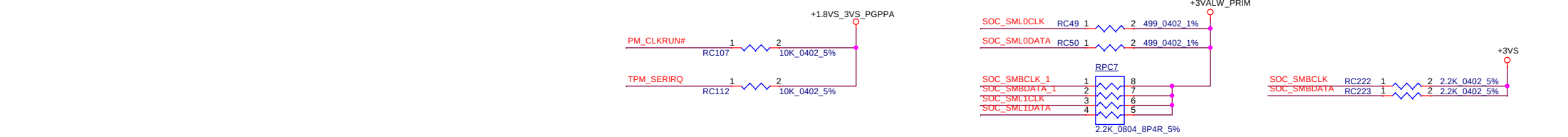
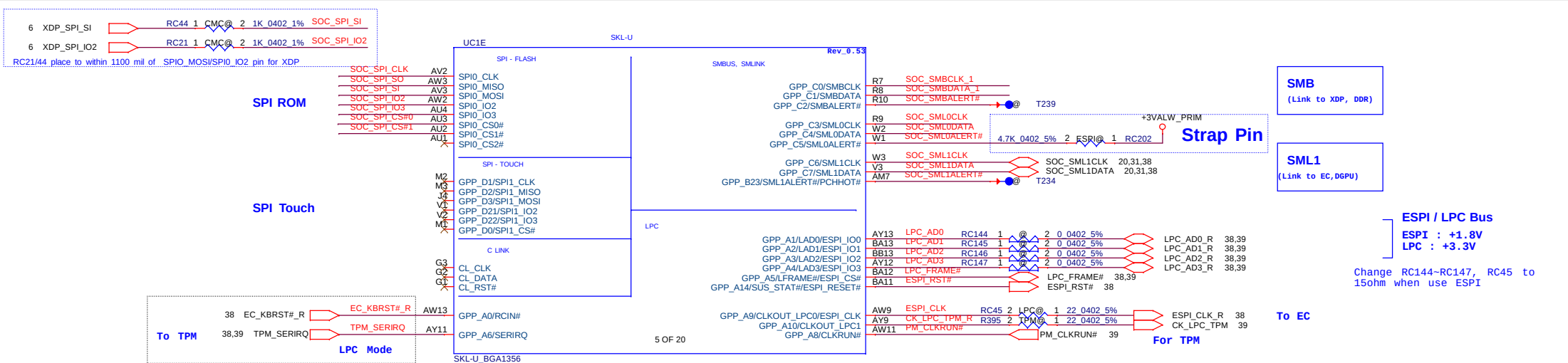


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				Document Number	
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Date: Monday June 22, 2015				Sheet	1 of 60

Interleaved Memory



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				SKL-U(2/12)DDRIII	
Size	Document Number			Rev	
	A4WAS M/B LA-C611P			1.0	
Date:	Tuesday, July 14, 2015	Sheet	7	of 60	



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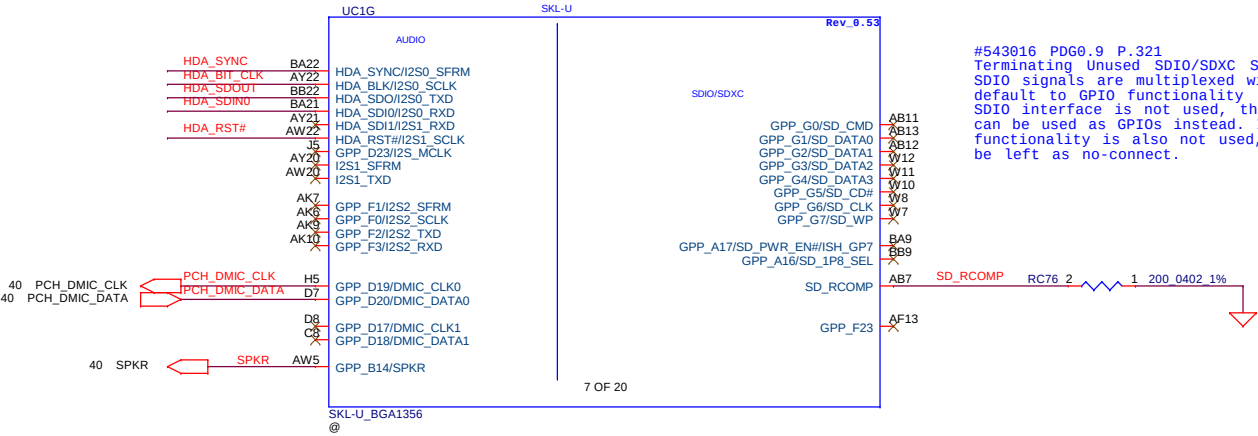
11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
 - SDO double pumped up to 48 Mb/s
 - SDT's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode.--> AAX05 Use
1 = Enable TOP Swap Mode.



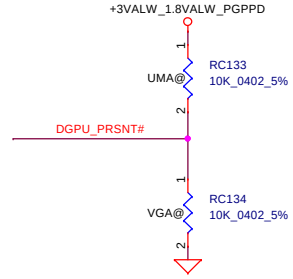
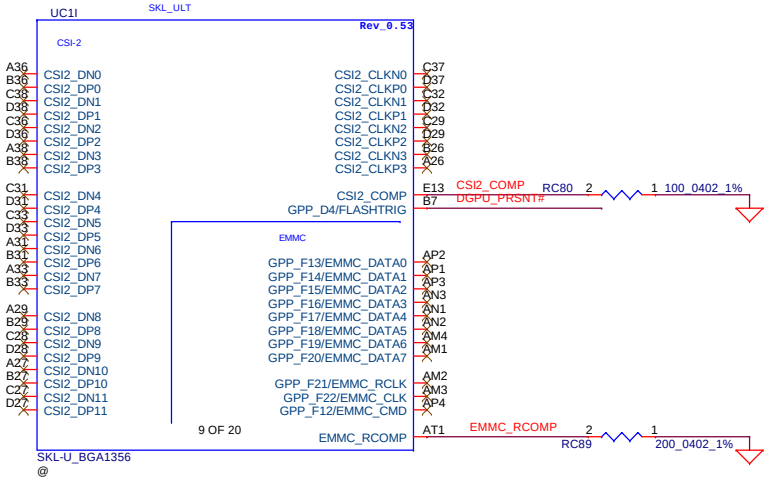
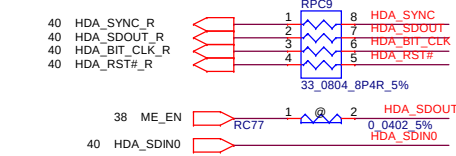
#543016 PDG0.9 P.321
Terminating Unused SDIO/SDXC Signals
SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDIO interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

62.3.38 RCOMP Checklist

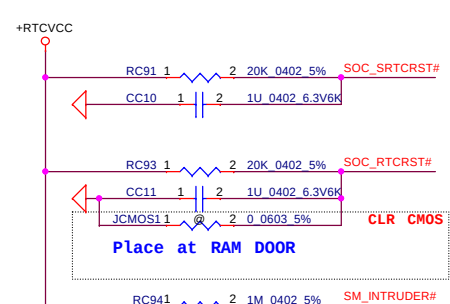
Table 62-48. RCOMP Checklist

Component	Value	✓
NOA_RCOMP	49.9 ohm +/- 1% pull down termination to GND	
FEQ_CCOMP	24.9ohm +/- 1% pull down termination to GND	
SD_RCOMP	200ohms termination to GND	
EHMC_RCOMP	200ohms termination to GND	
PCIE_RCOMP[R/N]	100 ohm +/- 1%. Differential between RCOMP/RCOMP#	
USM2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	
SD_RCOMP	200ohms termination to GND	
EHMC_RCOMP	200ohms termination to GND	
PCH_POPRCOMP	DC resistance <0.2ohm. 49.9 ohm termination resistor to GND.	
PCIE_RCOMP[R/N]	100 ohm +/- 1%. Differential between RCOMP/RCOMP#	
CSI2_COMP	100 ohm +/- 1% termination resistor to GND; DC resistance <0.5ohm.	
USM2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

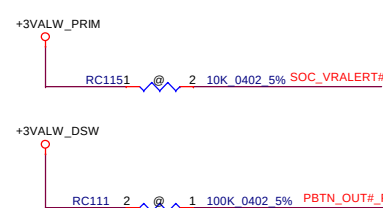
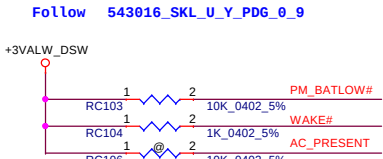
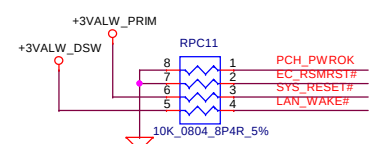
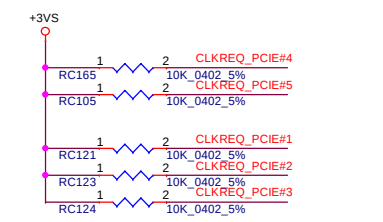
HDA for AUDIO



	GPIO67 DGPU_PRSNT#
DIS,Optimus	0
UMA	1



DGPU
PH at DGPU side
GLAN
NGFF WL+BT(KEY E)

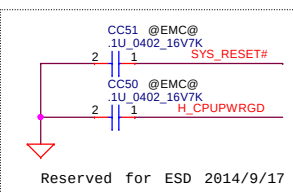
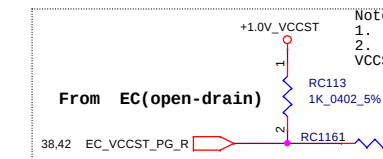


Note for PCH_PWROK
PDG1.0 Figure43-4 note20: PCH_PWROK
does not glitch when RSMRST# is
de-asserted

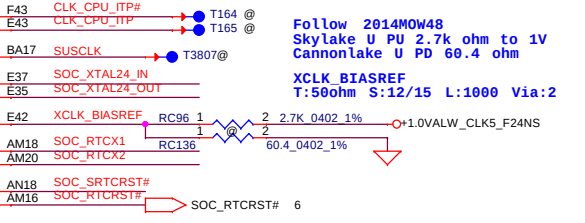
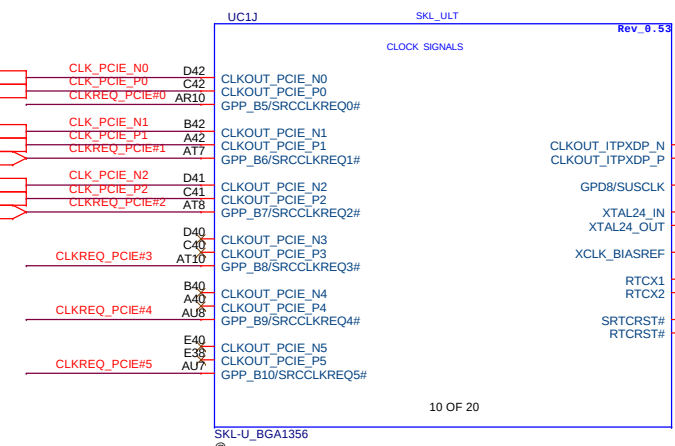
#543016 PDG0.9 P.526
PROC_PWRGD is used only for power sequence
debug and is not required to be connected to
anything on the platform.

WAKE# (DSX wake event)
10 K Ω pull-up to VccDSW3.3.
The pull-up is required even
if PCIe* interface is not
used on the platform.
LAN WAKE: LAN Wake Indicator from the GbE PHY.

Note for VCCST_PWRGD
1. 1.0V tolerance
2. PDG1.0 Figure43-4 note17: when failure events,
VCCST_PWRGD and PCH_PWROK de-assert at the same time



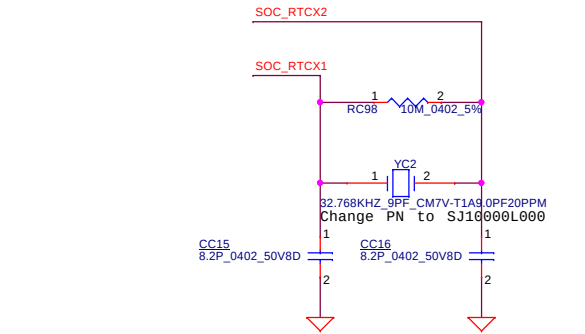
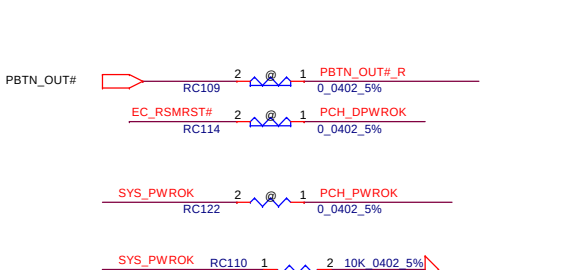
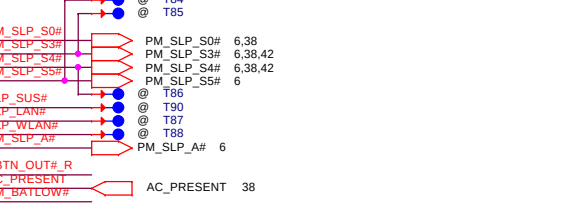
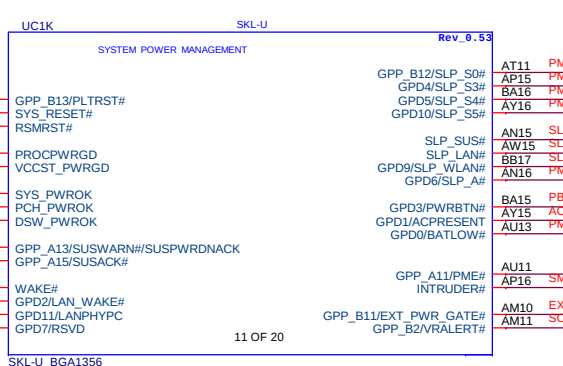
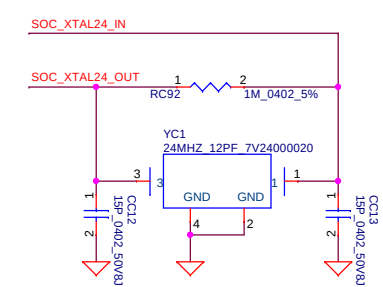
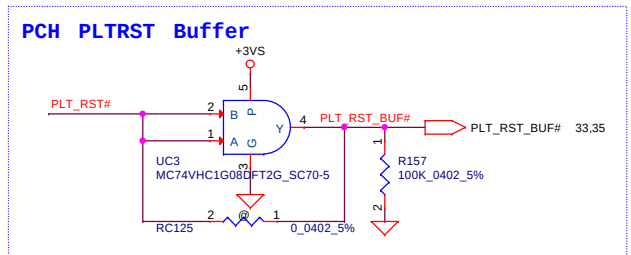
Reserved for ESD 2014/9/17



Follow 2014MOW48
Skylake U PU 2.7k ohm to 1V
Cannonlake U PD 60.4 ohm

XCLK_BIASREF
T:50ohm S:12/15 L:1000 Via:2

2014MOW48:
Skylake U use 24M 50 ohm ESR
Cannonlake U use 38.4M 30 ohm ESR



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						Size		Document Number		Rev	
						Custom		A4WAS M/B LA-C611P		1.0	
						Date:		Tuesday, June 16, 2015		Sheet 10 of 60	

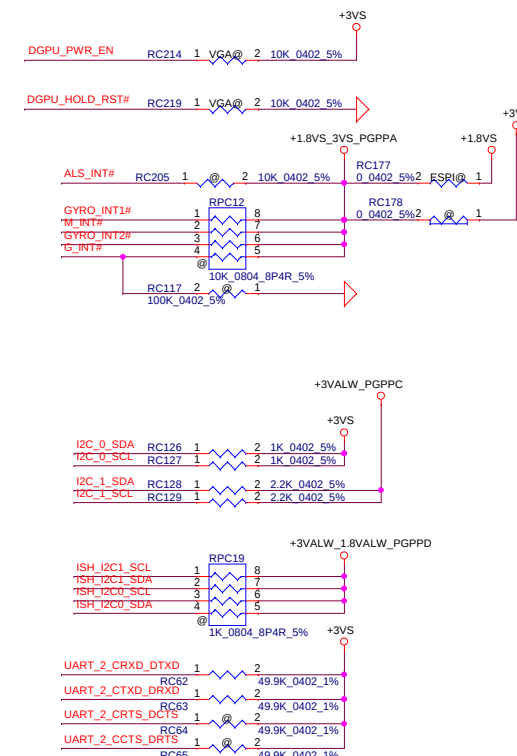


Figure 1: Embedded Location Elements

The diagram illustrates the architecture of an embedded location system, showing the interaction between an ISH (In-Sensor Hub) and a HOST, and the connection to various location and communication modules.

ISH (In-Sensor Hub) Components:

- I2C #0
- I2C #1
- I2C #2
- UART #1
- UART #0

HOST Components:

- UART_1
- I2C_5
- I2C_4
- UART_0

Control and Interface Blocks:

- SWI2 (I2C to ISH or HOST)
- SWI1 (UART to ISH or HOST)
- SWI2 (NGFF I2C to ISH UART or HOST I2C and one GPIO)
- GPIO Controller
- GPPI (11-10)
- GPPI (12-15)
- GPPI (11-8)
- NGFF Connector A-0P
- NGFF Connector A-0S

Location and Communication Modules:

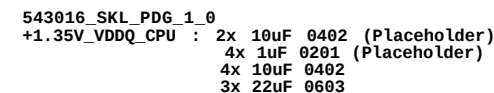
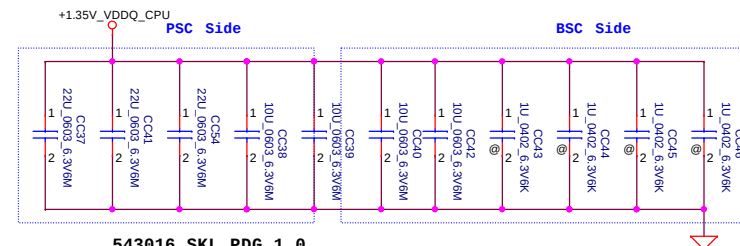
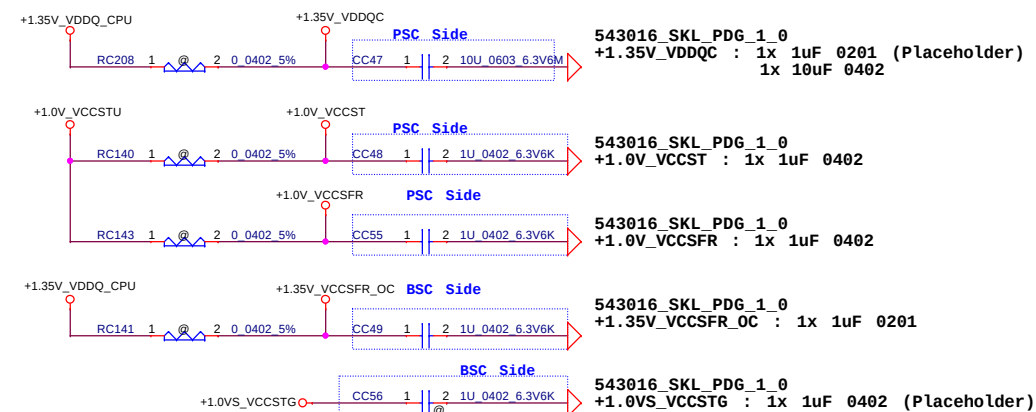
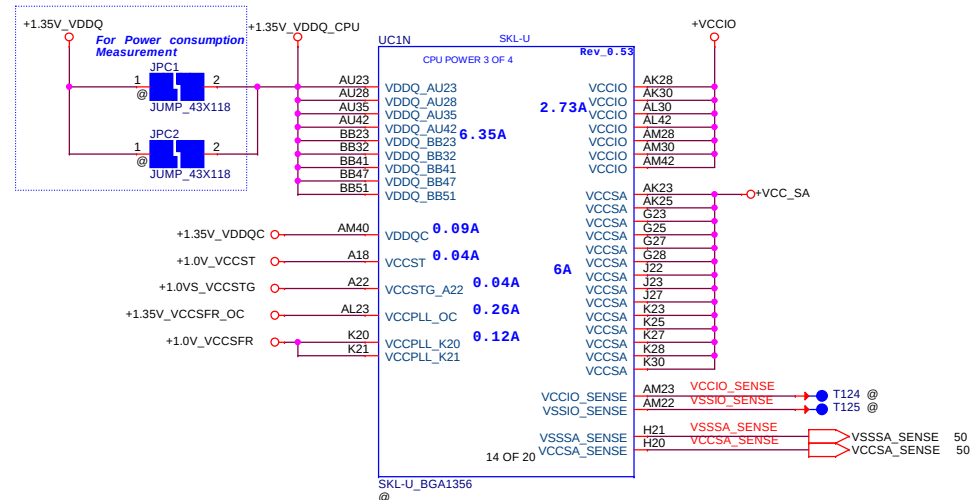
- 3G/LTE (XMM 726x)
- GNSS
- CG2000 GNSS
- BT (Bluetooth)
- WiFi

Legend:

- 3G
- WiFi
- BT
- GNSS

Note: If GNSS is part of GPS/MC it is already, but Snow GNSS would be disabled for embedded location usage.

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VCC 27A (U 15W Dual Core GT2)

+VCC CORE

UC1L SKL-U

+VCC CORE

VCCGT / VCCGTx(2+3e only) 40A(need confirm)

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

7.2.1.8 VCCGT VCC Specifications

VCCGT is a fixed 27A output voltage of 1.2V. The processor can draw 18 to 27A from VCCGT. Power Policy which sets 18 output to 27A using 27W signal as shown below:

Table 7-1. VCCGT Voltage Levels

State	VCCGT	18W
1	1.2	0
2	1.2	0

VCCGT Voltage Levels (Support only VCCGT)

Power State	Minimum Voltage	VCCGT Voltage	Notes
1	1.2	1.2	1
2	1.2	1.2	2
3	1.2	1.2	3

1. Processor can support 18W signal.

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

UC1L SKL-U

+VCC CORE

+VCC_GT

UC1M SKL-U

+VCC_GT

#544924 Skylake EDS P.125

VCCOPC 1V 2.8A

VCC_OPC_1P8 1.8V 50mA

VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

T132 @ VCCOPC_SENSE

T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE

T139 @ VSSEPIO_SENSE

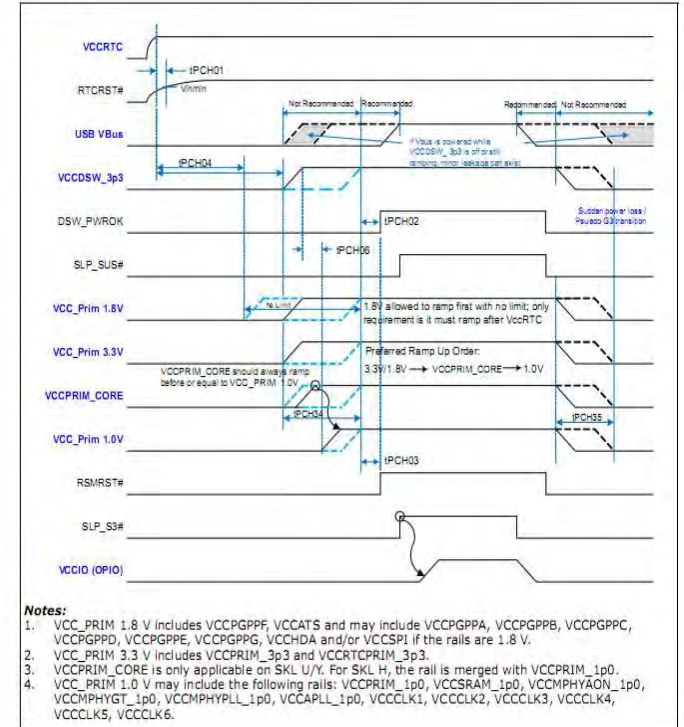
UC1L SKL-U

+VCC CORE

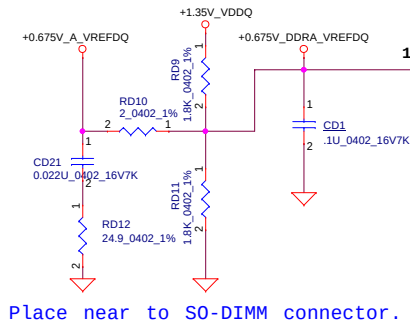
+V

UC1P SKL-U Rev. 0.53			UC1Q SKL-U Rev. 0.53			UC1R SKL-U Rev. 0.53				
GND 1 OF 3			GND 2 OF 3			GND 3 OF 3				
A5 VSS	AL65 VSS	AT63 VSS	BA49 VSS	F8 VSS	L18 VSS	SKL-U_BGA1356 @ 18 OF 20				
A67 VSS	AL66 VSS	AT68 VSS	BA53 VSS	G10 VSS	L2 VSS					
A70 VSS	AM13 VSS	AT71 VSS	BA57 VSS	G22 VSS	L20 VSS					
AA2 VSS	AM21 VSS	AU10 VSS	BA6 VSS	G43 VSS	L4 VSS					
AA4 VSS	AM25 VSS	AU15 VSS	BA62 VSS	G45 VSS	L8 VSS					
AA65 VSS	AM27 VSS	AU20 VSS	BA66 VSS	G48 VSS	N10 VSS					
AA68 VSS	AM43 VSS	AU32 VSS	BA71 VSS	G5 VSS	N13 VSS					
AB15 VSS	AM45 VSS	AU38 VSS	BB18 VSS	G52 VSS	N19 VSS					
AB16 VSS	AM46 VSS	AV1 VSS	BB26 VSS	G55 VSS	N21 VSS					
AB18 VSS	AM55 VSS	AV68 VSS	BB30 VSS	G58 VSS	N6 VSS					
AB21 VSS	AM60 VSS	AV69 VSS	BB34 VSS	G6 VSS	N65 VSS					
AB8 VSS	AM61 VSS	AV70 VSS	BB38 VSS	G60 VSS	N68 VSS					
AD13 VSS	AM68 VSS	AV71 VSS	BB43 VSS	G63 VSS	P17 VSS					
AD16 VSS	AM71 VSS	AW10 VSS	BB55 VSS	G66 VSS	P19 VSS					
AD19 VSS	AM8 VSS	AW12 VSS	BB6 VSS	H15 VSS	P20 VSS					
AD20 VSS	AN20 VSS	AW14 VSS	BB60 VSS	H18 VSS	P21 VSS					
AD21 VSS	AN23 VSS	AW16 VSS	BB64 VSS	H71 VSS	R13 VSS					
AD62 VSS	AN28 VSS	AW18 VSS	BB67 VSS	J11 VSS	R6 VSS					
AD8 VSS	AN30 VSS	AW21 VSS	BB70 VSS	J13 VSS	T15 VSS					
AE64 VSS	AN32 VSS	AW23 VSS	C1 VSS	J25 VSS	T17 VSS					
AE65 VSS	AN33 VSS	AW26 VSS	C25 VSS	J28 VSS	T18 VSS					
AE66 VSS	AN35 VSS	AW28 VSS	C5 VSS	J32 VSS	T2 VSS					
AE67 VSS	AN37 VSS	AW30 VSS	D10 VSS	J35 VSS	T21 VSS					
AE68 VSS	AN38 VSS	AW32 VSS	D11 VSS	J38 VSS	T4 VSS					
AE69 VSS	AN40 VSS	AW34 VSS	D14 VSS	J42 VSS	U10 VSS					
AF1 VSS	AN42 VSS	AW36 VSS	D18 VSS	J8 VSS	U63 VSS					
AF10 VSS	AN58 VSS	AW38 VSS	D22 VSS	K16 VSS	U64 VSS					
AF15 VSS	AN63 VSS	AW41 VSS	D25 VSS	K18 VSS	U66 VSS					
AF17 VSS	AP10 VSS	AW43 VSS	D26 VSS	K22 VSS	U67 VSS					
AF2 VSS	AP18 VSS	AW45 VSS	D30 VSS	K61 VSS	U69 VSS					
AF4 VSS	AP20 VSS	AW47 VSS	D34 VSS	K63 VSS	U70 VSS					
AF63 VSS	AP23 VSS	AW49 VSS	D39 VSS	K64 VSS	V16 VSS					
AG16 VSS	AP28 VSS	AW51 VSS	D44 VSS	K65 VSS	V17 VSS					
AG17 VSS	AP32 VSS	AW53 VSS	D45 VSS	K66 VSS	V18 VSS					
AG18 VSS	AP35 VSS	AW55 VSS	D47 VSS	K67 VSS	W13 VSS					
AG19 VSS	AP38 VSS	AW57 VSS	D48 VSS	K68 VSS	W6 VSS					
AG20 VSS	AP42 VSS	AW6 VSS	D53 VSS	K70 VSS	W9 VSS					
AG21 VSS	AP58 VSS	AW60 VSS	D58 VSS	K71 VSS	Y17 VSS					
AG71 VSS	AP63 VSS	AW62 VSS	D6 VSS	L11 VSS	Y19 VSS					
AH13 VSS	AP68 VSS	AW64 VSS	D62 VSS	L16 VSS	Y20 VSS					
AH6 VSS	AP70 VSS	AW66 VSS	D66 VSS	L17 VSS	Y21 VSS					
AH63 VSS	AR11 VSS	AW8 VSS	D69 VSS	E11 VSS	SKL-U_BGA1356 @ 17 OF 20					
AH64 VSS	AR15 VSS	AY66 VSS	E15 VSS	E18 VSS						
AH67 VSS	AR16 VSS	B10 VSS	E21 VSS	E21 VSS						
AJ15 VSS	AR20 VSS	B14 VSS	E46 VSS	E46 VSS						
AJ18 VSS	AR23 VSS	B18 VSS	E50 VSS	E50 VSS						
AJ20 VSS	AR28 VSS	B22 VSS	E53 VSS	E53 VSS						
AJ4 VSS	AR35 VSS	B30 VSS	E56 VSS	E56 VSS						
AK11 VSS	AR42 VSS	B34 VSS	E6 VSS	E6 VSS						
AK16 VSS	AR43 VSS	B39 VSS	E65 VSS	E65 VSS						
AK18 VSS	AR45 VSS	B44 VSS	E71 VSS	E71 VSS						
AK21 VSS	AR46 VSS	B48 VSS	F1 VSS	F1 VSS						
AK22 VSS	AR48 VSS	B53 VSS	F13 VSS	F13 VSS						
AK27 VSS	AR5 VSS	B58 VSS	F2 VSS	F2 VSS						
AK63 VSS	AR50 VSS	B62 VSS	F22 VSS	F22 VSS						
AK68 VSS	AR52 VSS	B66 VSS	F23 VSS	F23 VSS						
AK69 VSS	AR53 VSS	B71 VSS	F27 VSS	F27 VSS						
AK8 VSS	AR55 VSS	BA1 VSS	F28 VSS	F28 VSS						
AL2 VSS	AR58 VSS	BA10 VSS	F32 VSS	F32 VSS						
AL28 VSS	AR63 VSS	BA14 VSS	F33 VSS	F33 VSS						
AL32 VSS	AR6 VSS	BA18 VSS	F35 VSS	F35 VSS						
AL35 VSS	AT2 VSS	BA2 VSS	F37 VSS	F37 VSS						
AL38 VSS	AT20 VSS	BA23 VSS	F38 VSS	F38 VSS						
AL4 VSS	AT23 VSS	BA28 VSS	F4 VSS	F4 VSS						
AL45 VSS	AT28 VSS	BA32 VSS	F40 VSS	F40 VSS						
AL48 VSS	AT35 VSS	BA36 VSS	F42 VSS	F42 VSS						
AL52 VSS	AT4 VSS	F68 VSS	BA41 VSS	BA41 VSS						
AL55 VSS	AT42 VSS	BA45 VSS								
AL58 VSS	AT56 VSS									
AL64 VSS	AT58 VSS									

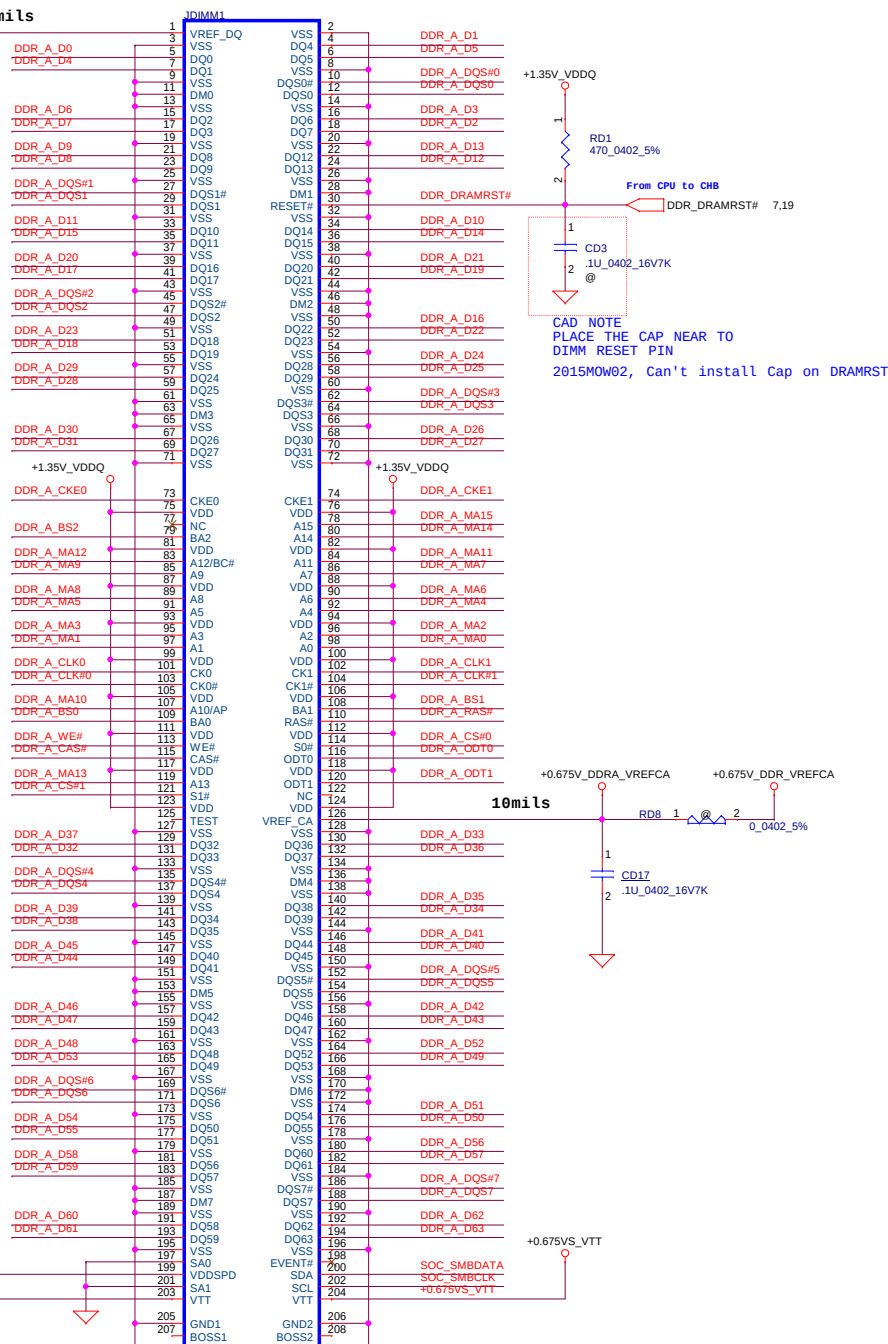
Figure 46-18.SKL-U/Y Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System



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Size Custom		Document Number		Rev 1.0	
Date: Tuesday, June 16, 2015		Sheet 16 of 60		A4WAS M/B LA-C611P	

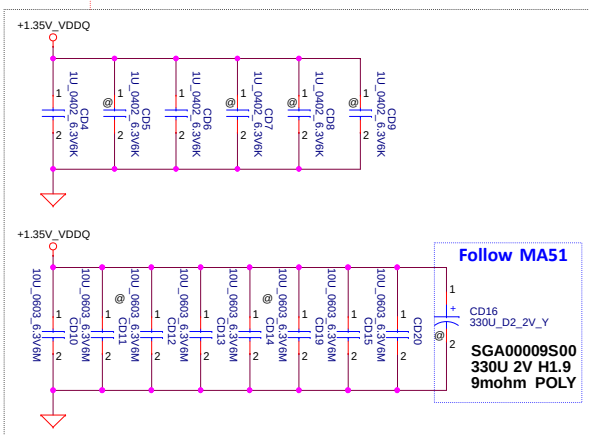


Place near to SO-DIMM connector.



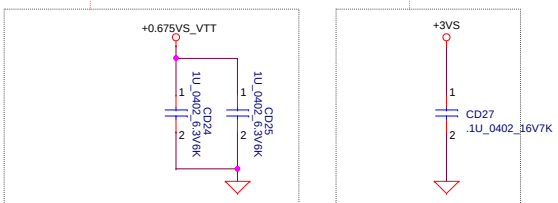
Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF DQ at the DIMM socket



Layout Note:
Place near JDIMM1.203,204

Layout Note:
Place near JDIMM1.199

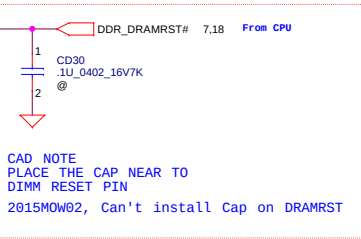
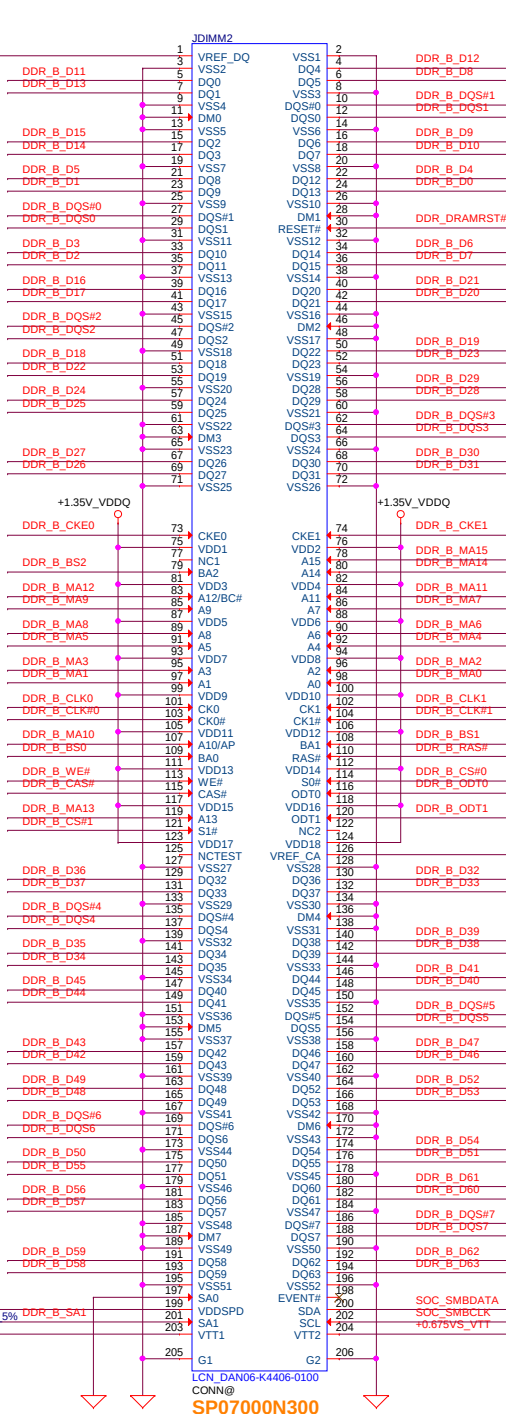
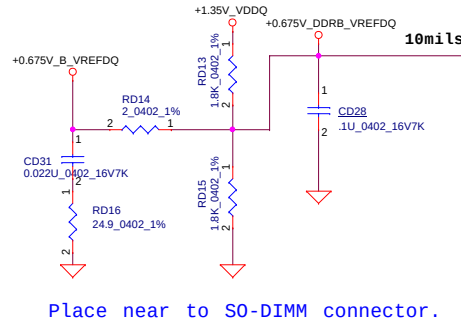
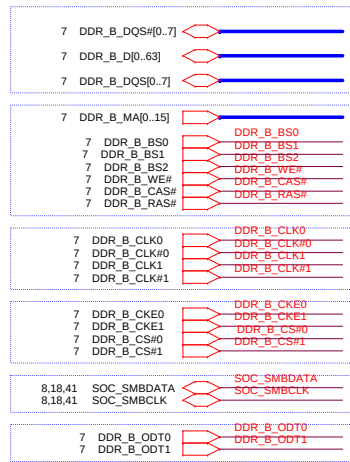


Interleaved Memory

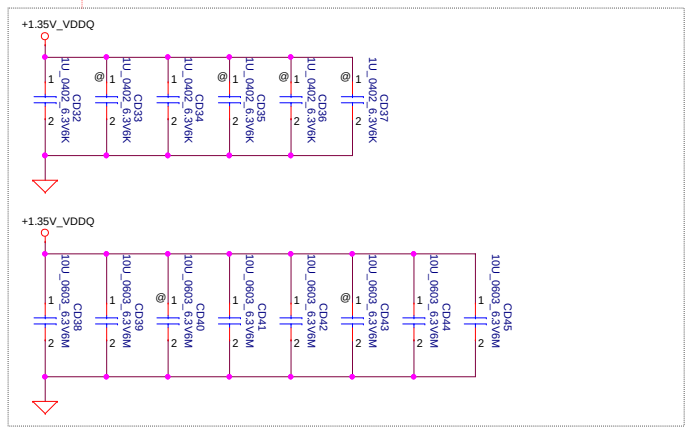
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				Size	Document	Number	Rev	
				Custom		A4WAS M/B LA-C611P	1.0	
Date:				Tuesday, June 16, 2015	Sheet	18 of 60		

Standard Type

2-3A to 1 DIMMs/channel

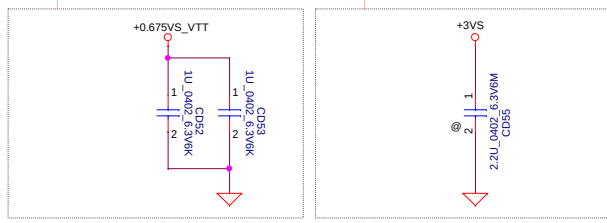


Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204

Layout Note:
Place near JDIMM2.199



Place near to S0-DIMM connector.

Interleaved Memory

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						Size		Document Number		A4WAS M/B LA-C611P		Rev 1.0	
						Custom							
						Date:		Tuesday, June 16, 2015		Sheet 19 of 60			

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				Date:	Tuesday, June 16, 2015	Sheet

38mA

SM010019400 3300mA 330ohm@100mhz DCR 0.05

+PLLVD

1 C2003
VGA@
2 Z2U_0603 6.3V6M

Near GPU

1 L2000
CHILISIN PB160808T-350Y-N

2 VGA@

+1.05VSDGPU

17mA

SM01000AG00 2A 300ohm@100mhz DCR 0.1

+GPU_PLLVD

1 C2006
10U_0603 6.3V6M
2 VGA@

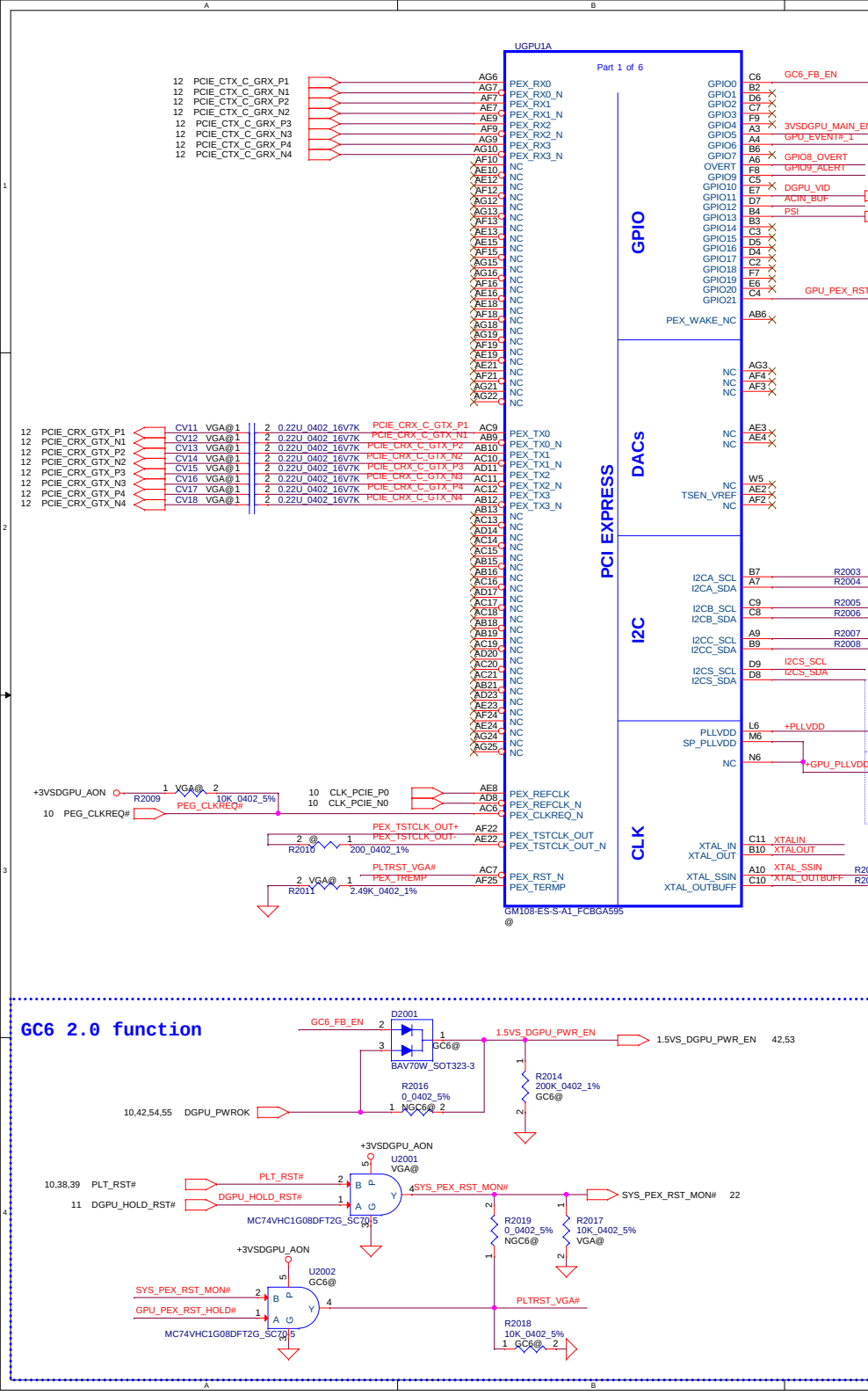
Near GPU

1 C2007
47U_0805 6.3V6M

2 VGA@

1 L2001
HCB1608KF-301T20P

2 VGA@



38mA

SM010019400 3300mA 330ohm@100mhz DCR 0.05

+PLLVD

1 C2003
VGA@
2 Z2U_0603 6.3V6M

Near GPU

1 L2000
CHILISIN PB160808T-350Y-N

2 VGA@

+1.05VSDGPU

17mA

SM01000AG00 2A 300ohm@100mhz DCR 0.1

+GPU_PLLVD

1 C2006
10U_0603 6.3V6M
2 VGA@

Near GPU

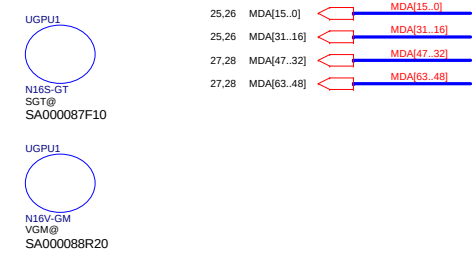
1 C2007
47U_0805 6.3V6M

2 VGA@

1 L2001
HCB1608KF-301T20P

2 VGA@

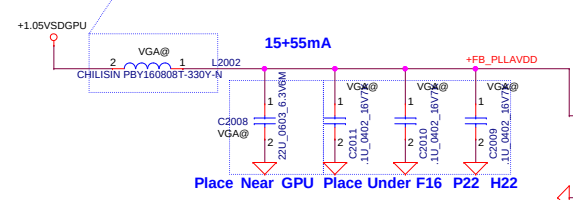
VRAM Interface



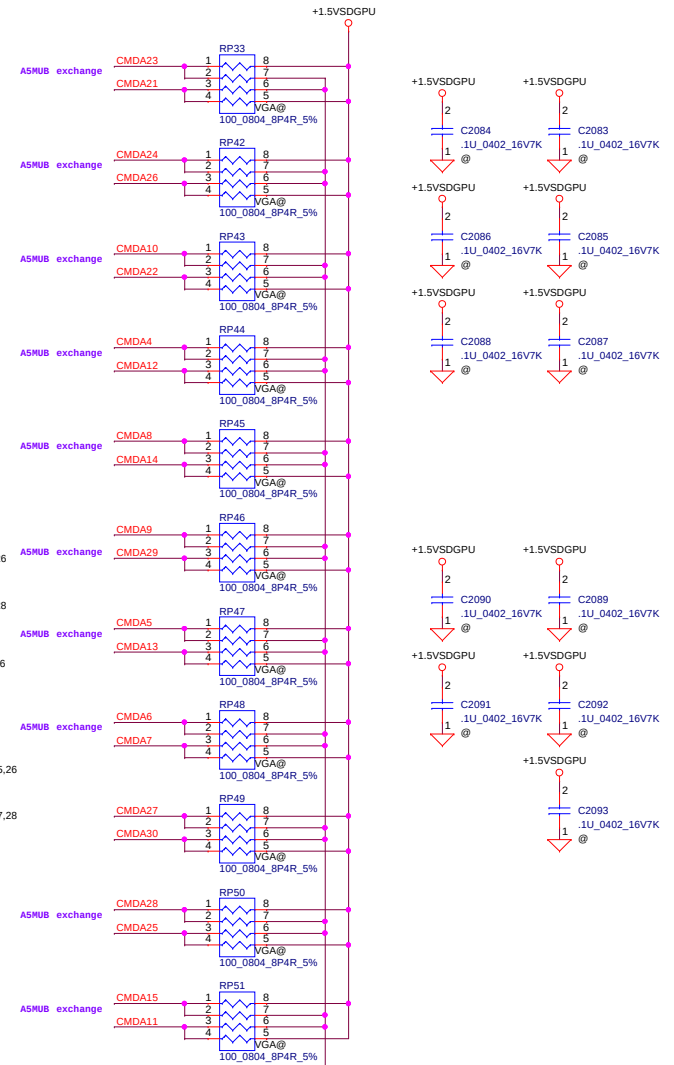
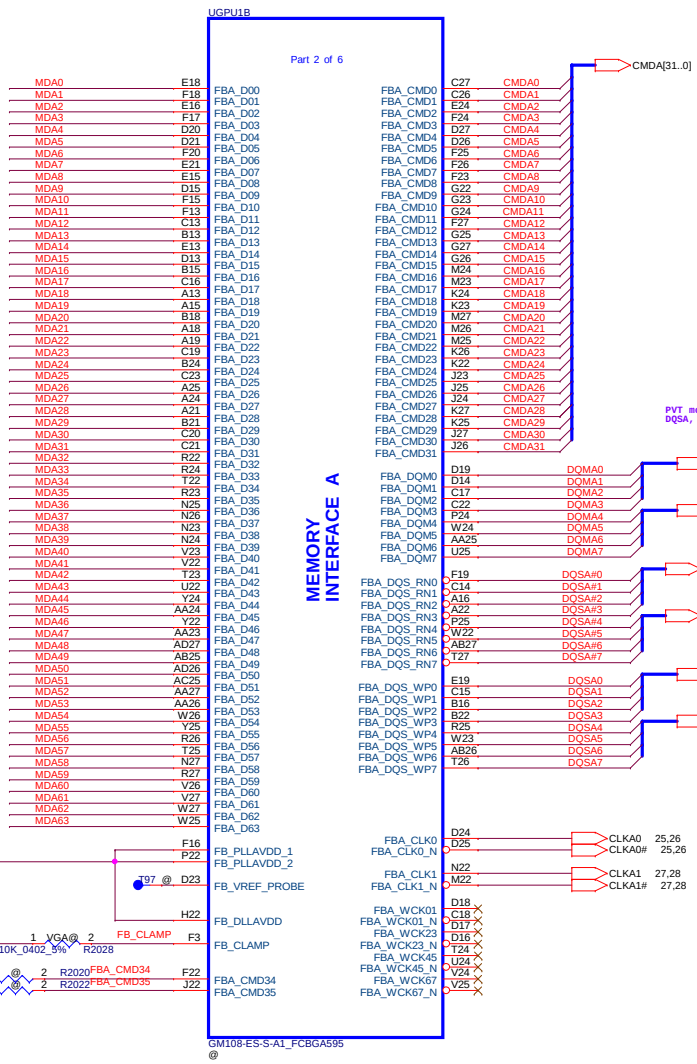
NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 μ F	X7R	0402	2	Under GPU
		22 μ F	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM010019400 3000ma 33ohm@100mhz DCR 0.05



change to 1.35VSDGPU



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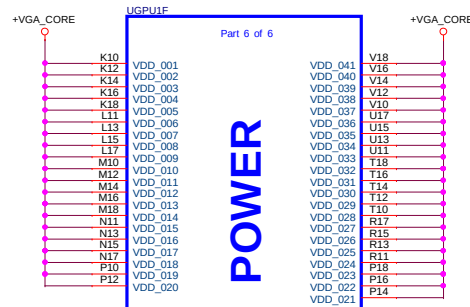
GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1 μ F X7R	0402	2 2	Under GPU
	1 μ F X7R	0603	2 2	Under GPU
	4.7 μ F X6S	0603	2 2	Under GPU
	10 μ F X5R	0805	1 1	Near GPU
	22 μ F X5R	0805	1 1	Near GPU

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0 μ F X6S	0402	1	Under GPU
	4.7 μ F X6S	0603	1	Near GPU
	10 μ F X5R	0805	1	Midway between GPU and Power Supply
	22 μ F X5R	0805	1	Midway between GPU and Power Supply

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
G82B-64 GB4B-128 GB3-256	3V3_MAIN	0.1 μ F	X6S	0402	2	2	Under GPU
		1 μ F	X5R	0603	1	1	Near GPU
		4.7 μ F	X5R	0603	1	1	Near GPU
G82B-64 GB4B-128 GB3-256		0.1 μ F	X6S	0402	1	1	Under GPU
		1 μ F	X5R	0603	1	1	Near GPU
		4.7 μ F	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μ F	X5R	0402	1	Near GPU
4.7 μ F	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μ F	X6S	0402	1	Under GPU
1.0 μ F	X5R	0603	1	Near GPU
4.7 μ F	X5R	0805	1	Near GPU



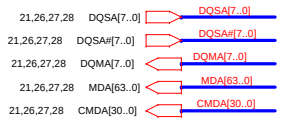
GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 μ F	X6S	0603	10	10	Under GPU	
	1 μ F	X6S	0402	4	4	Under GPU	
	47 μ F	X5R	0805	1	1	Near GPU	
	22 μ F	X5R	0805	1	1	Near GPU	
	4.7 μ F	X5R	0805	5	5	Near GPU	
	330 μ F	POS	7343	1	1	Near GPU	ESR ≤ 6 m Ω

		GPU Core	FB Total	1.05V Total
		—	1.5/1.35V	1.05V
Products	VRM Type	(A)	(A)	(A)
H155-GM	DDR3/L	48.11	4.23	0.91
H155-GT	DDR3/L	60.07	4.26	0.91

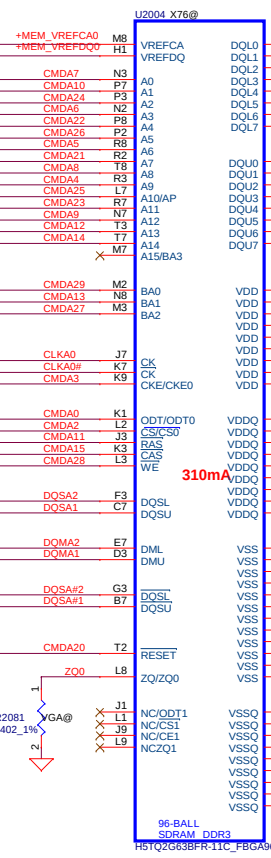
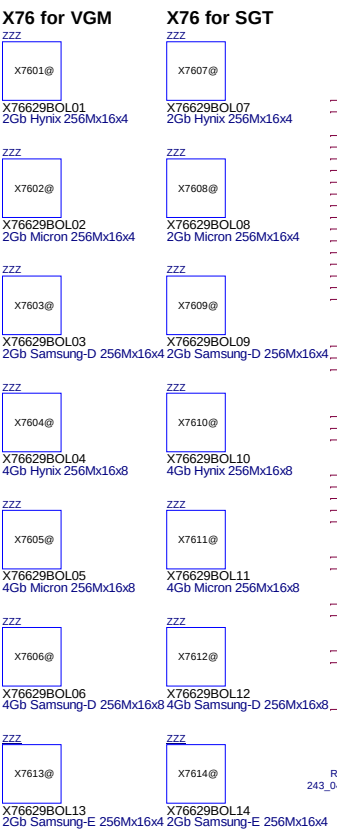
Power Supply Rail	N15V-GM-5
(V)	DDR3/L
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

	N15V-GL
Power Supply Rail	DDR3
(V)	(A)
GPU Core Max.	28.26
FB Total	4.07
PEXVDD	1.82

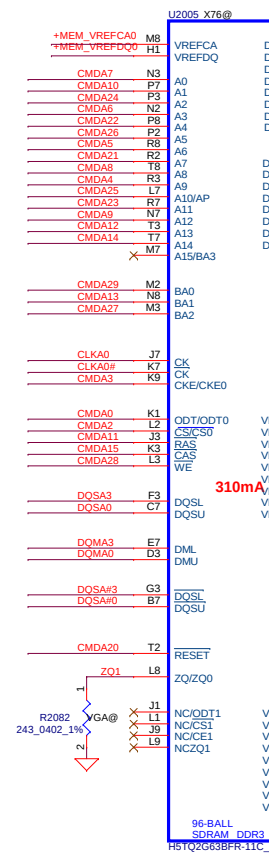
VRAM DDR3 chips



Lower Rank 0 BOT SIDE



310mA



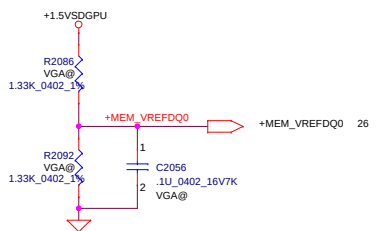
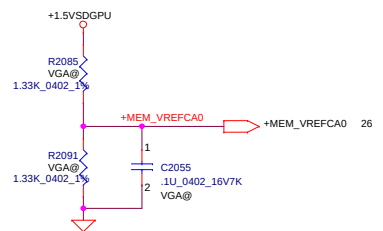
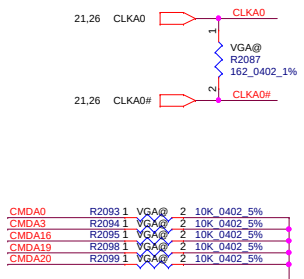
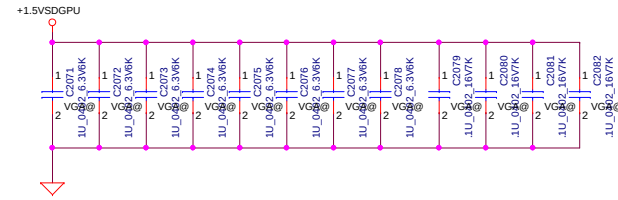
310mA

Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST		
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

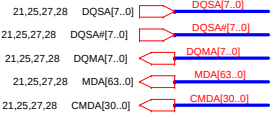
DDR3	Command Bit	Default Pull-down
	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

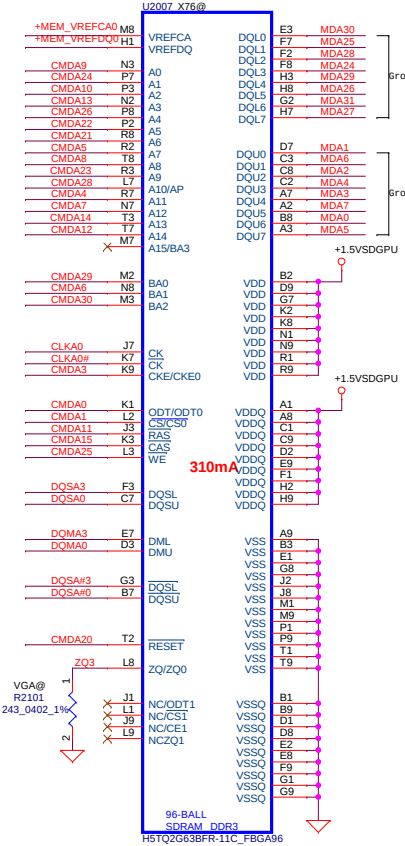
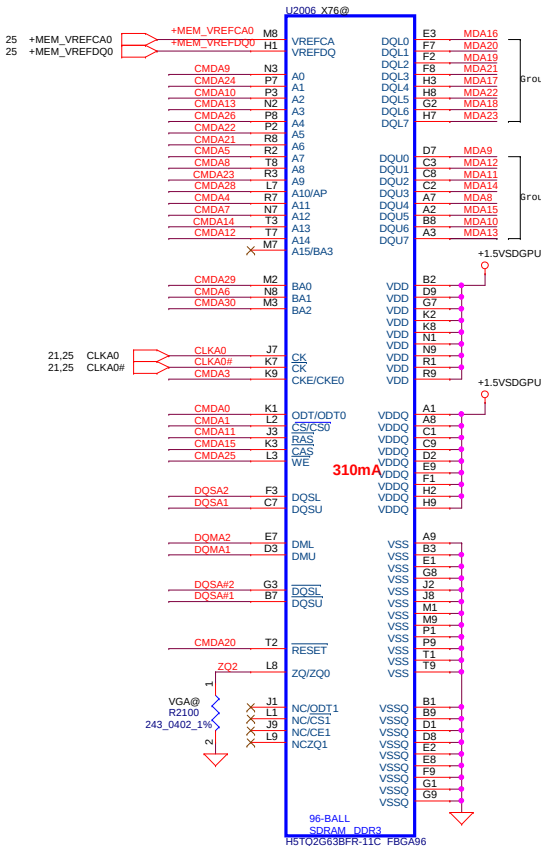
Capacitor Type		Population		Location
FBVDD/Q Combined		FBVDDQ	FBVDD	
0.1 µF	X7R	0402	2	Under DRAM
1.0 µF	X7R	0603	4	Under DRAM
10 µF	X5R	0805	0	Close to DRAM



VRAM DDR3 chips

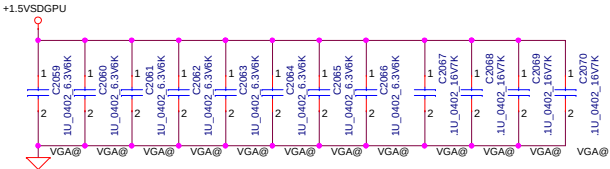


Lower Rank 1 TOP SIDE

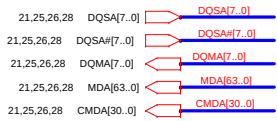


Mode E Address	Rank0		Rank1	
	0...31	32..63	0...31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

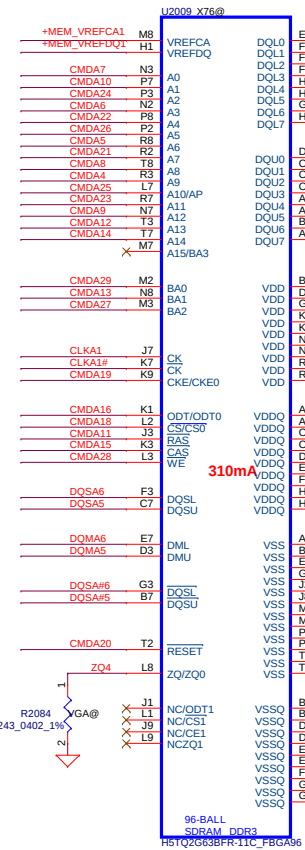
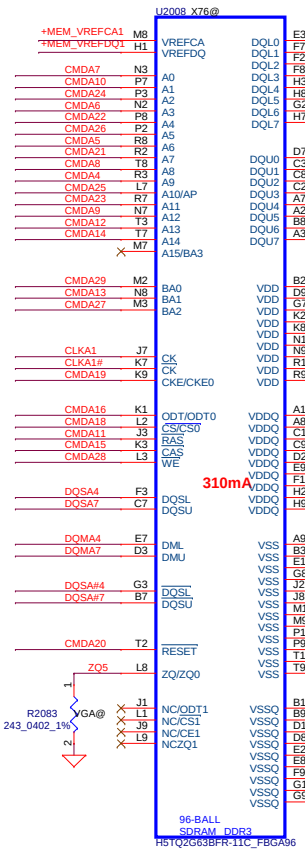
DDR3	Command Bit	Default Pull-down
	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



VRAM DDR3 chips

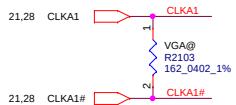
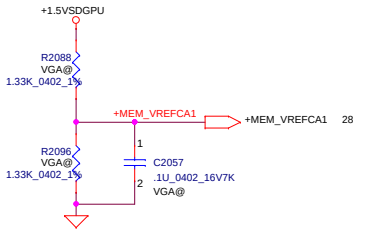
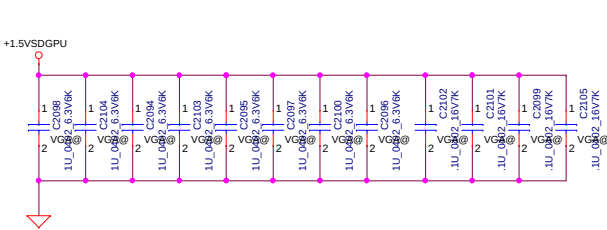


Upper Rank 0 BOT SIDE

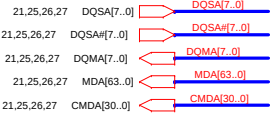


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

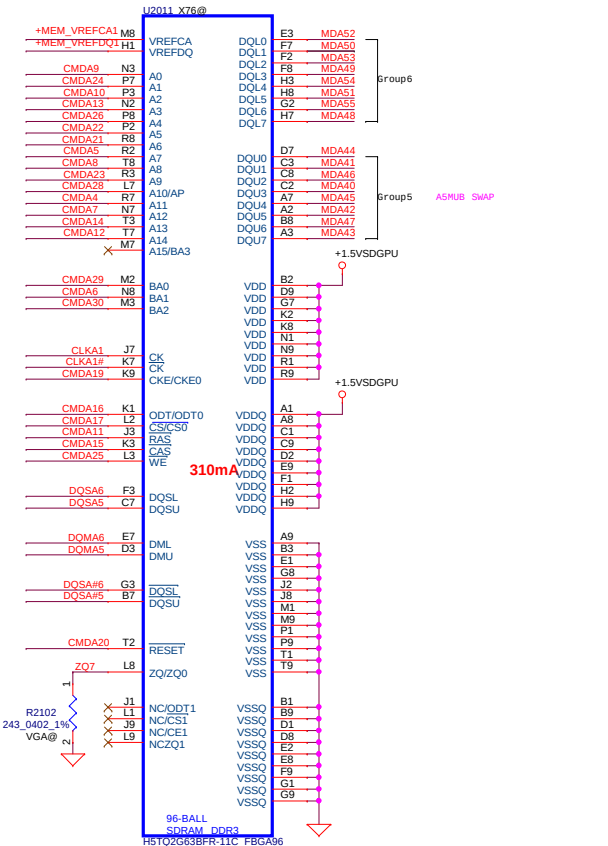
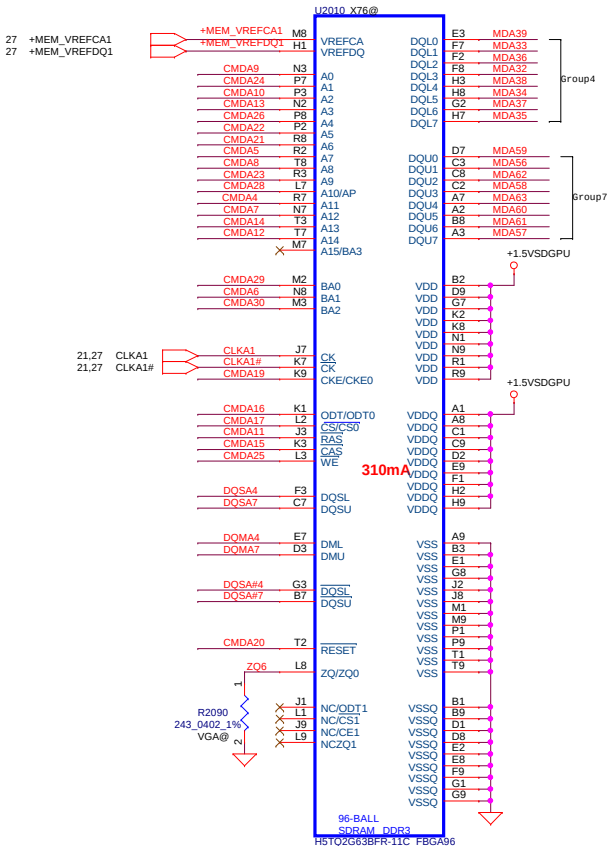
DDR3	Command Bit	Default Pull-down
	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



VRAM DDR3 chips

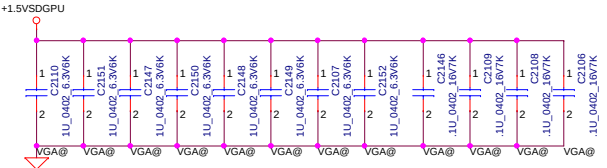


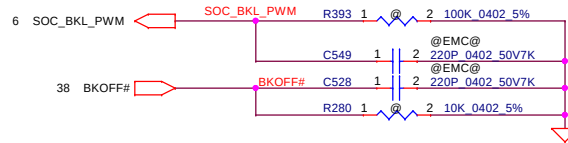
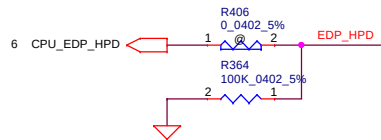
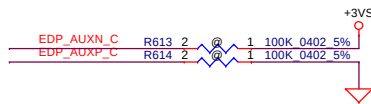
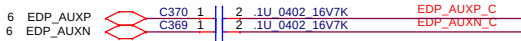
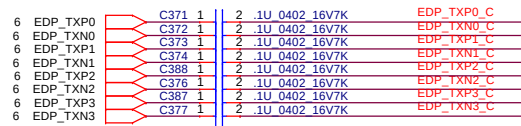
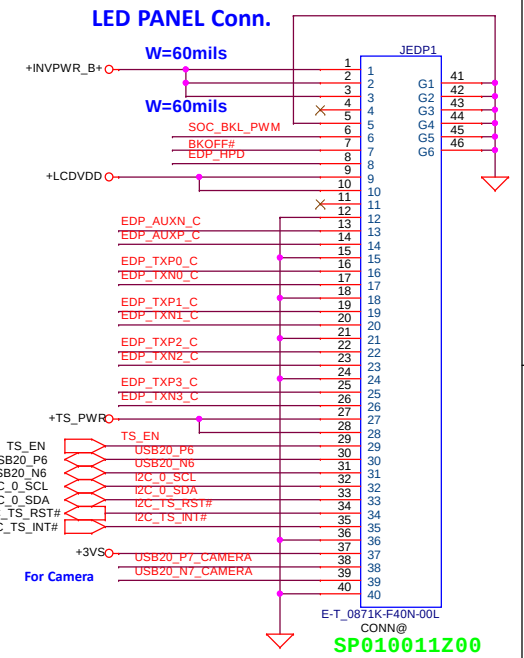
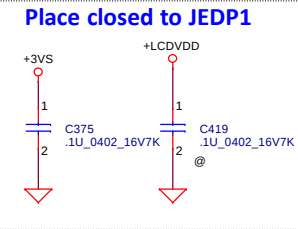
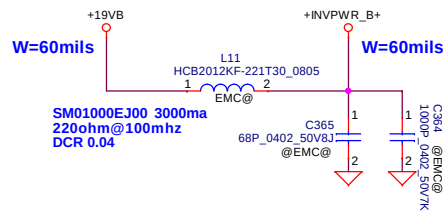
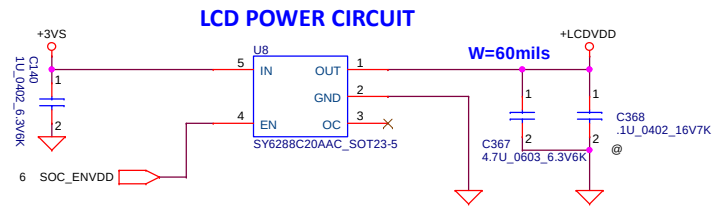
Upper Rank 1 TOP SIDE



Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT			
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

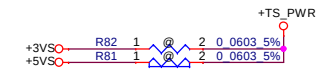
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



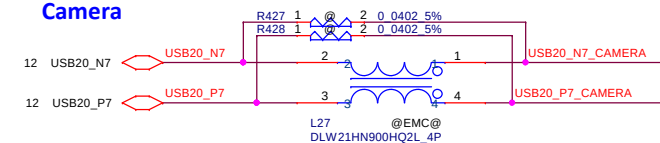


Touch Screen

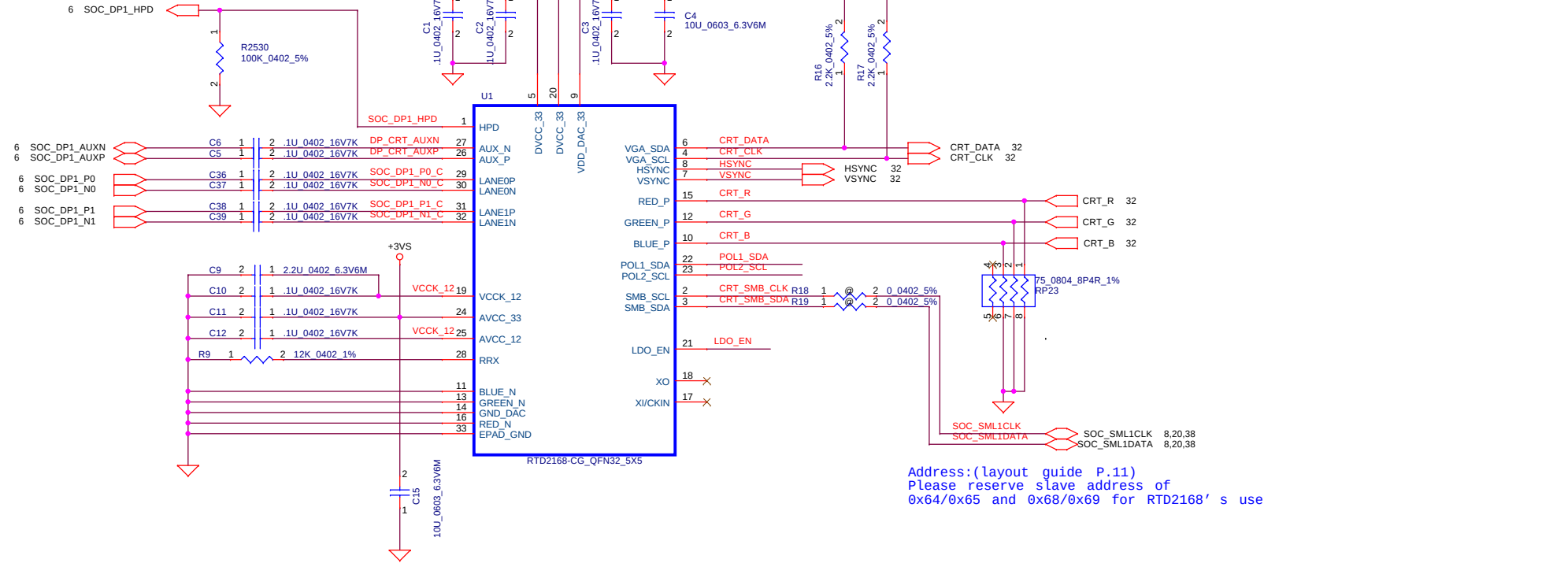
I2C Touch Screen



Camera



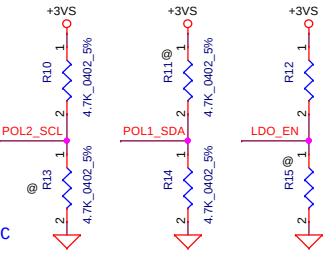
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2014/11/10		Deciphered Date		2016/11/10		Title			
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						Size Custom		Document Number		Rev 1.0	
						A4WAS M/B LA-C611P					
						Date: Tuesday, June 16, 2015		Sheet 29 of 60			



Address:(layout guide P.11)
Please reserve slave address of
0x64/0x65 and 0x68/0x69 for RTD2168' s use

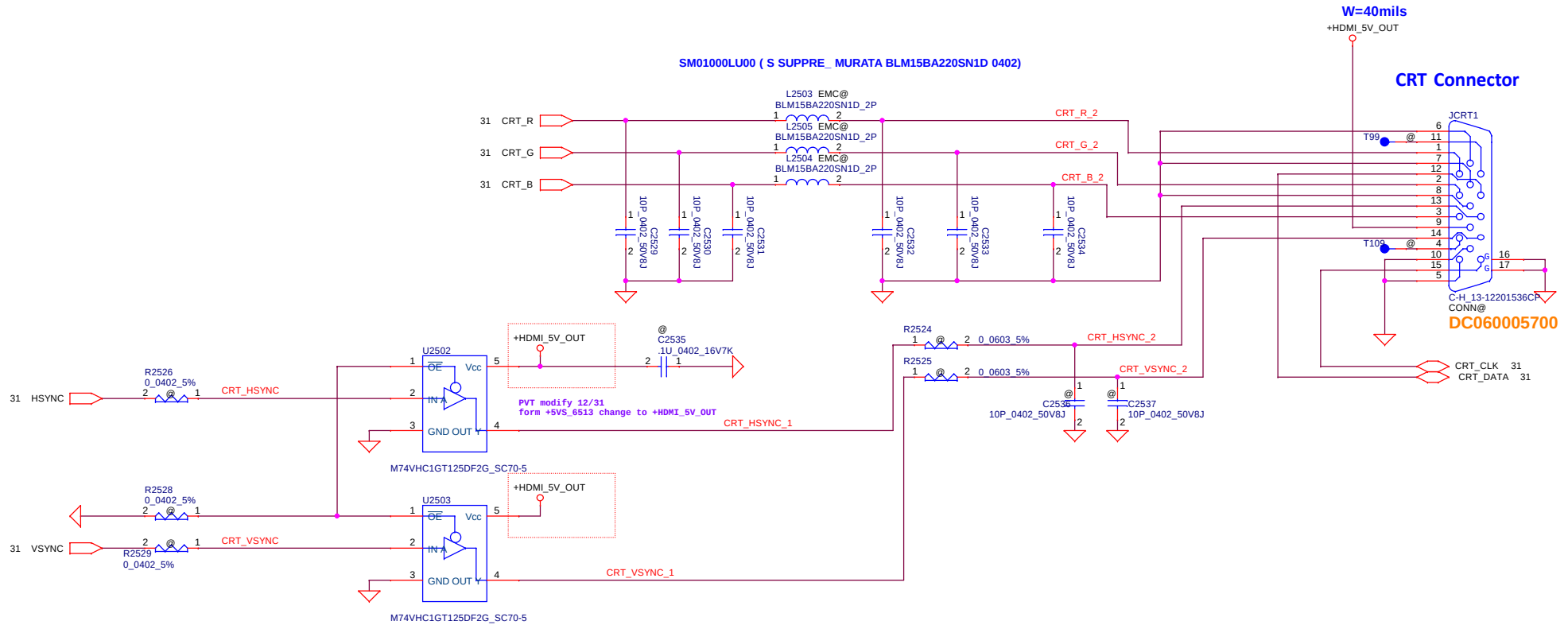
		POL_SDA	
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM



LDO_EN:
*1: Internal 1.2V
0: External 1.2V

CRT conn.



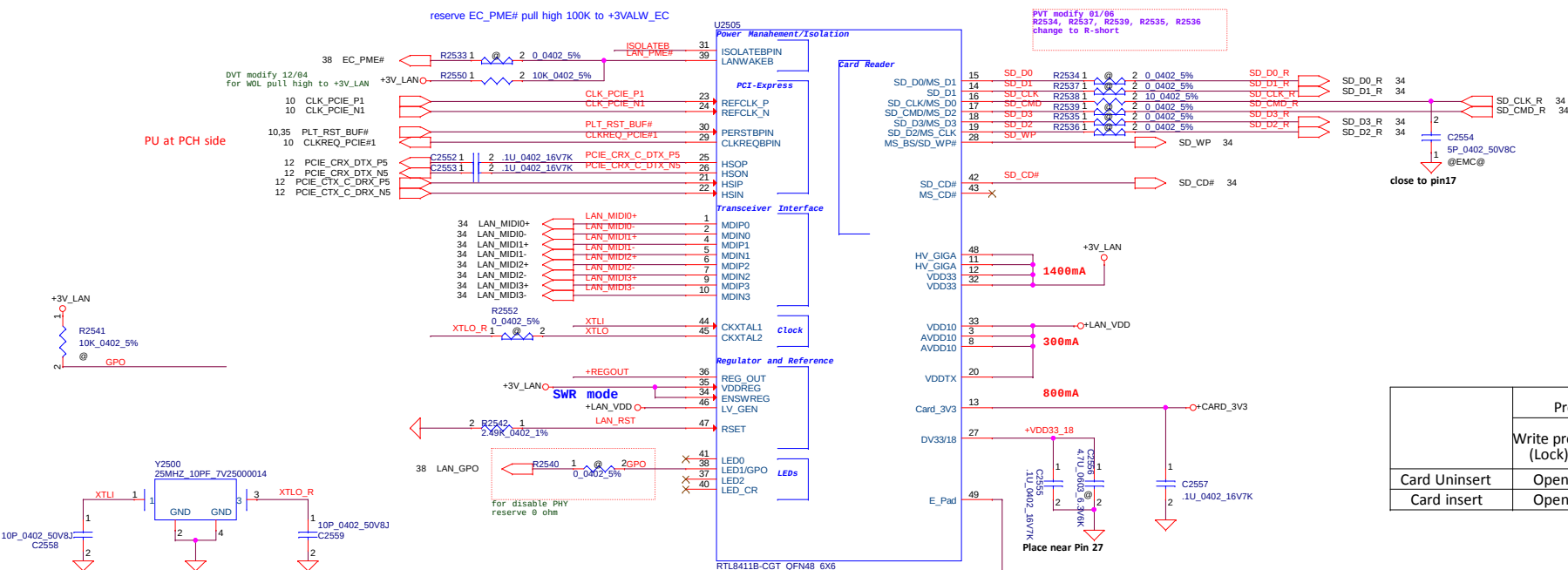
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2014/11/10		Deciphered Date		2016/11/10		Title			
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						Size Custom		Document Number		Rev 1.0	
						Date:		Tuesday, June 16, 2015		Sheet 32 of 60	
						A4WAS M/B LA-C611P					

W=60mil

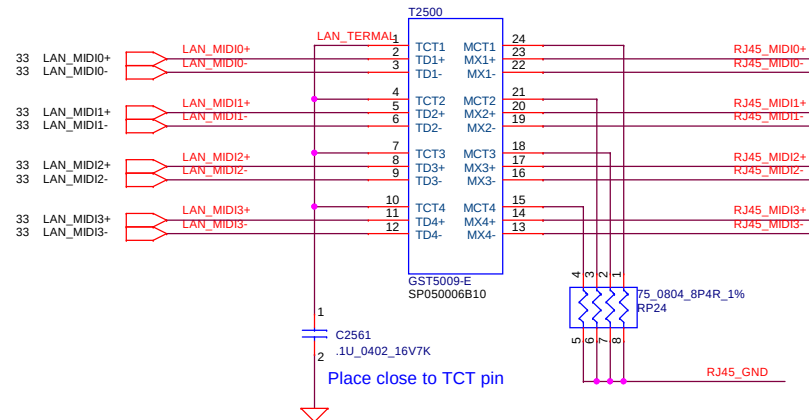
11/27: P/N change to SH00000RT00
(S COIL 2.2UH +-20%
HPC252012NF-2R2M 1.3A)

```
Using for Switch mode
The trace length
from C to
PIN34, 35(VDDREG)
must < 200mils.
```

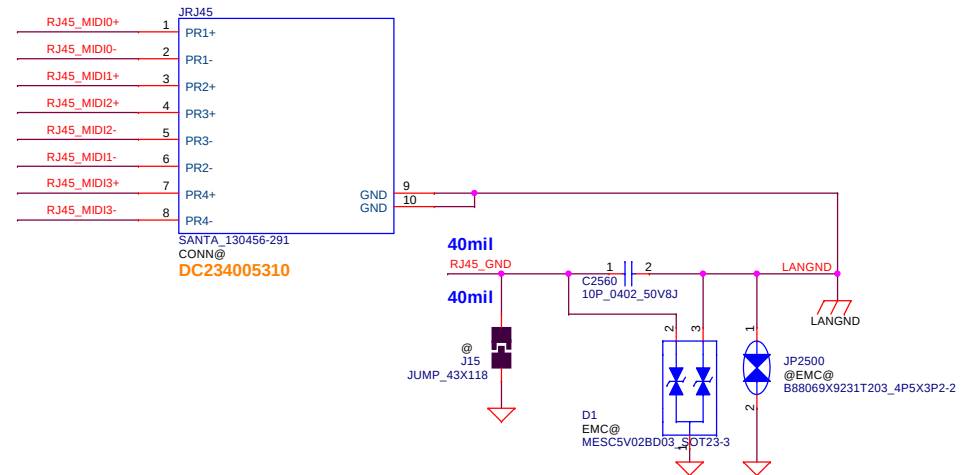
Place near Pin 11,32,48



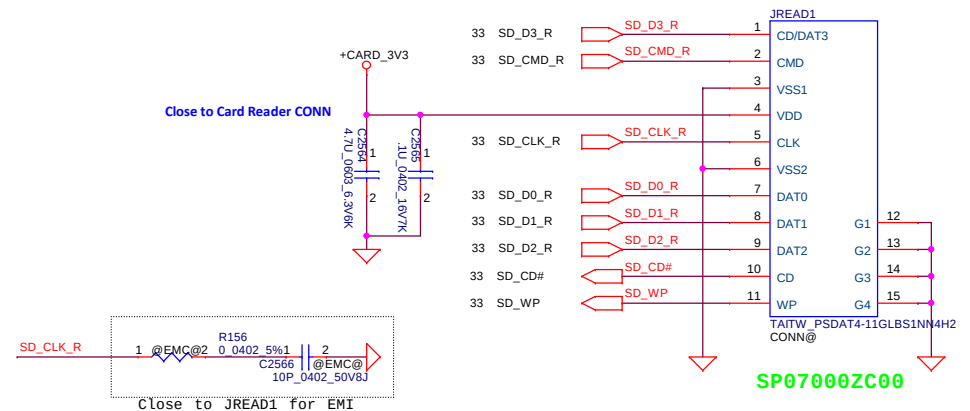
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close



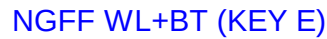
LAN Connector



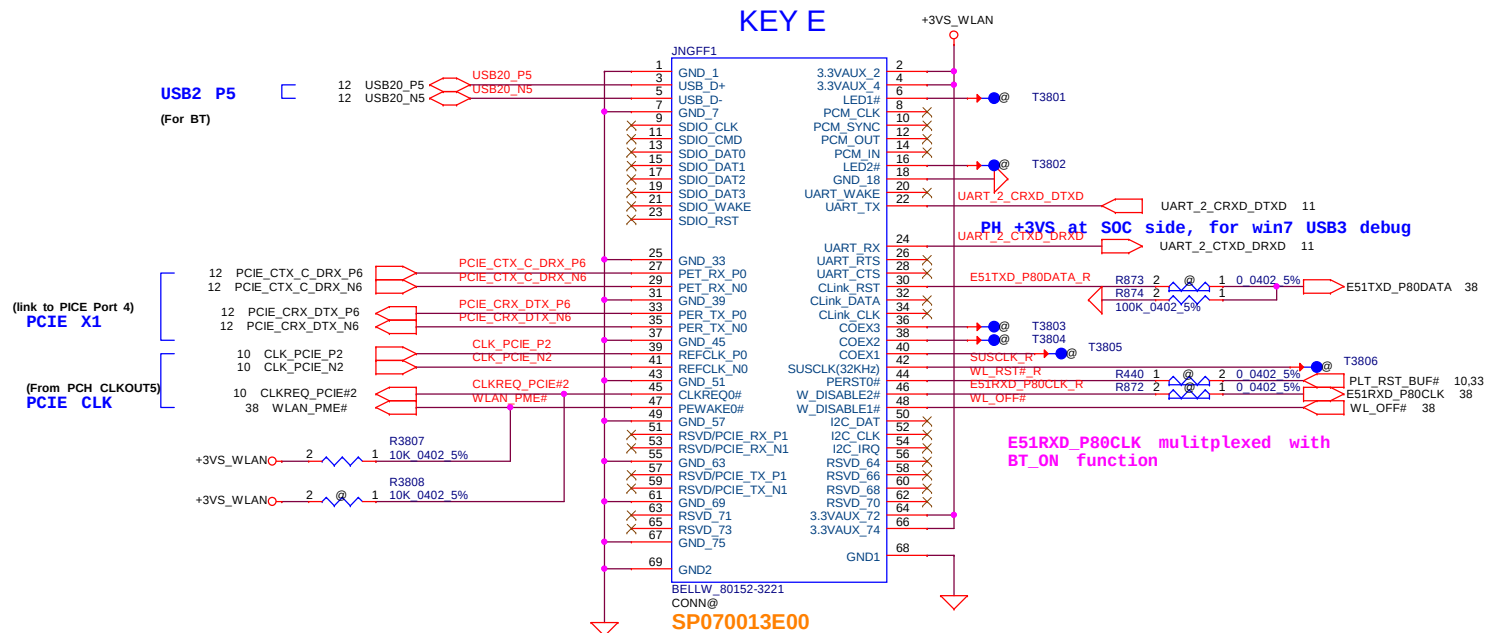
Card Reader Connector



Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2014/11/10		Deciphered Date		2016/11/10		Title			
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						Size		Document Number		Rev	
						Custom		A4WAS M/B LA-C611P		1.0	
						Date:		Tuesday, June 16, 2015		Sheet 34 of 60	



74	2-pin	GPIO	75
72	3-pin	RESERVED/REFCLK1	73
70	UMI_Power_SMC/GPIO/PEWake#	RESERVED/REFCLK1	71
68	UMI_Power_SMC/CLKREQ1	GPIO	69
66	UMI_SWP_PERSIST	Reserved/PEFm1	67
64	RESERVED	Reserved/PEPm1	65
62	ALERT0 (IO/D3.3)	GPIO	63
60	DCCLK (IO/D3.3)	Reserved/PTm1	61
58	QC DATA (IO/D3.3)	Reserved/PTp1	59
56	W_DISABLE1 (IO/D3.3V)	GPIO	57
54	Reserved/W_DISABLE1 (IO/D3.3V)	PEWake0 (IO/D3.3V)	55
52	PESTON (IO/D3.3V)	CLKREQ0 (IO/D3.3V)	53
50	SUSCLK30Hz (IO/D3.3V)	GPIO	51
48	CODE1 (IO/D1.8V)	REFCLK0	49
46	CODE2 (IO/D1.8V)	REFCLK0	47
44	CODE3 (IO/D1.8V)	GPIO	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GPIO	39
36	UART1T0 (IO/D1.8V)	PETr0	37
34	UART1T1 (IO/D1.8V)	PETr0	35
32	UART1T2 (IO/D1.8V)	GPIO	33
30	UART1T3 (IO/D1.8V)	GPIO	31
28	UART1T4 (IO/D1.8V)	GPIO	29
26	UART1T5 (IO/D1.8V)	GPIO	27
24	UART1T6 (IO/D1.8V)	GPIO	25
22	UART1T7 (IO/D1.8V)	GPIO	23
20	UARTWake# (IO/D3.3V)	SDIO Wake# (IO/D1.8V)	21
18	GPIO	SDIO Data7 (IO/D1.8V)	19
16	LED2 (I/O/D)	SDIO Data7 (IO/D1.8V)	17
14	PCMC_WAKE/DS_DS_OUT (IO/D1.8V)	SDIO Data7 (IO/D1.8V)	15
12	PCMC_WAKE/DS_DS_IN (IO/D1.8V)	SDIO CMD0 (IO/D1.8V)	13
10	PCMC_SYNC/DS_DS (IO/D1.8V)	SDIO CMD0 (IO/D1.8V)	11
8	PCMC_CLK/DS_SCK (IO/D1.8V)	SDIO CMD0 (IO/D1.8V)	9
6	LED1 (I/O/D)	GPIO	7
4	2-pin	USB_D-	5
2	2-pin	USB_D+	3
		GPIO	1

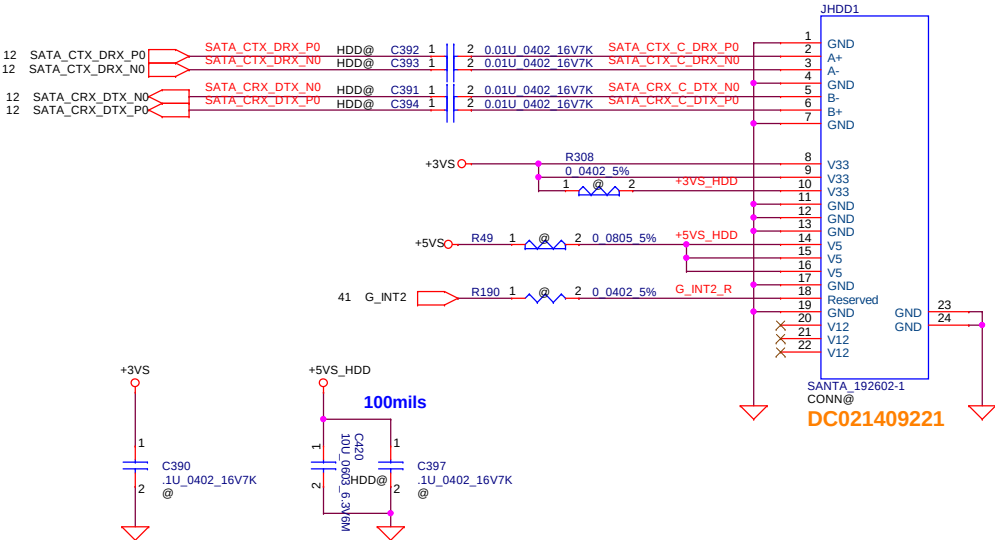


The UART power management protocol supports the following 4-wire and 5-wire interfaces:

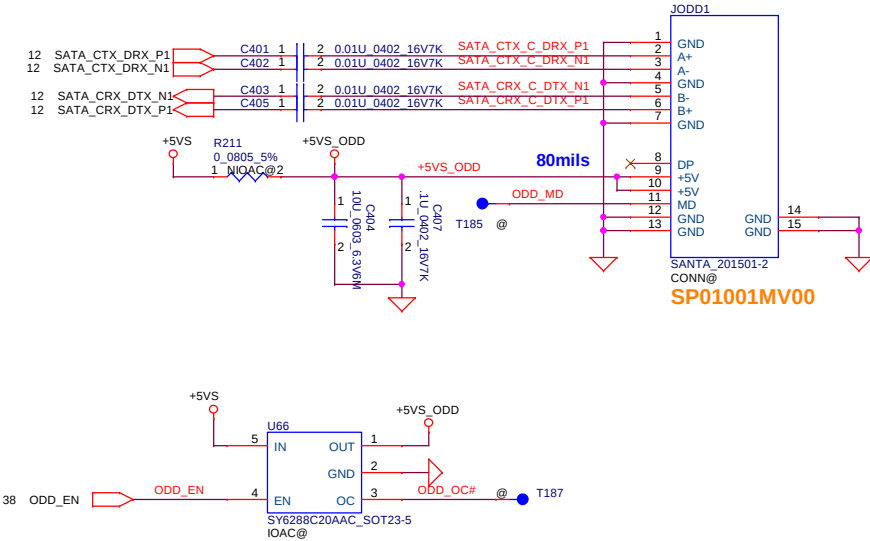
- ❑ ~~HDX~~ **UART_RXD** (Input): Receive Data
- ❑ ~~HTX~~ **UART_TXD** (Output): Transmit Data
- ❑ **UART_RTS** (Input): Request to Send (Host Flow Control)
- ❑ **UART_CTS** (Output): Clear to Send (Device Flow Control)
- ❑ ~~Host Wake-Up~~ **UART_Wake#** (Output): Host wake-up line is optional in case the host support in band wake-up

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Issued Date		2014/11/10	Deciphered Date		2016/11/10	Title		
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						Size	Document Number	Rev
						Custody	A4WAS M/B LA-C611P	1.0
						Date:	Tuesday, June 16, 2015	Sheet 35 of 60

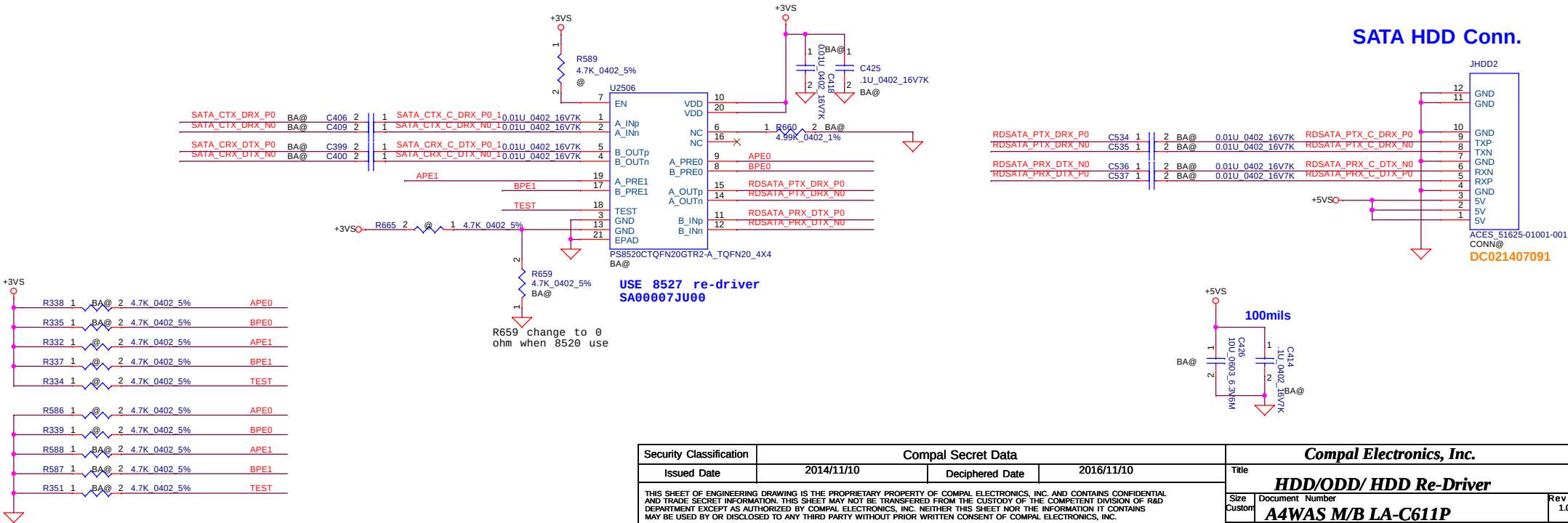
SATA HDD Conn.



SATA ODD Conn.

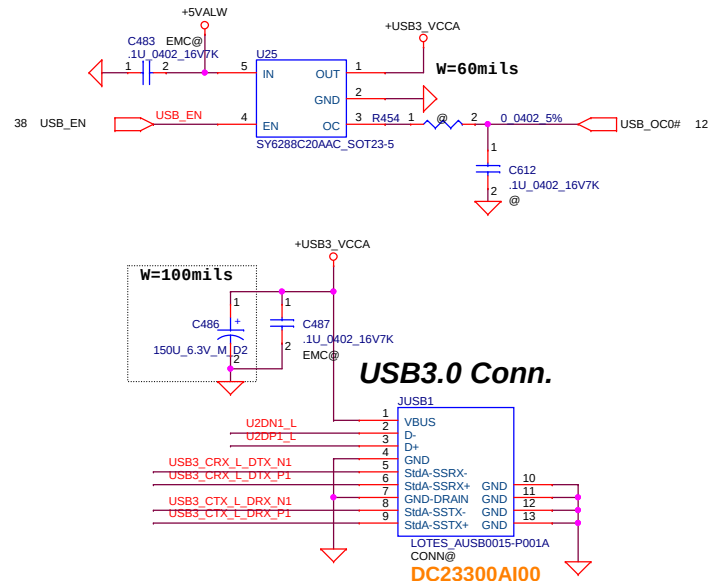
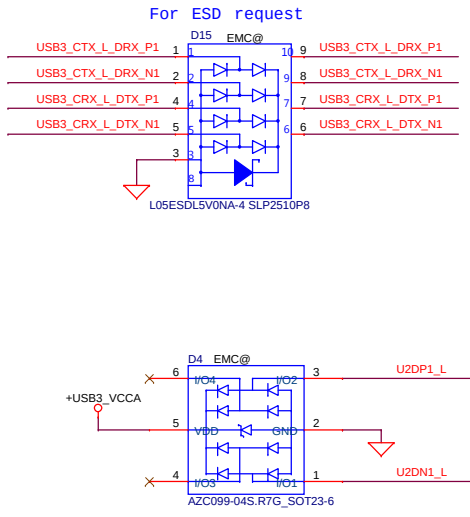
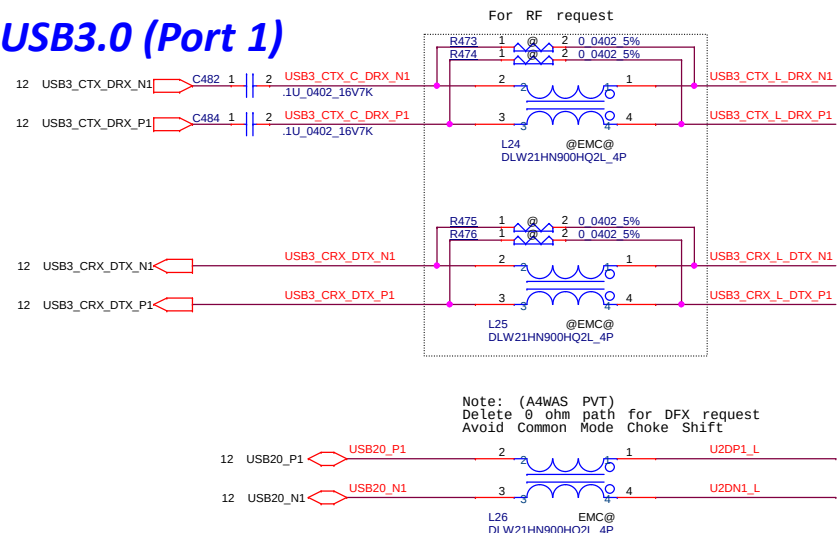


SATA HDD Conn.

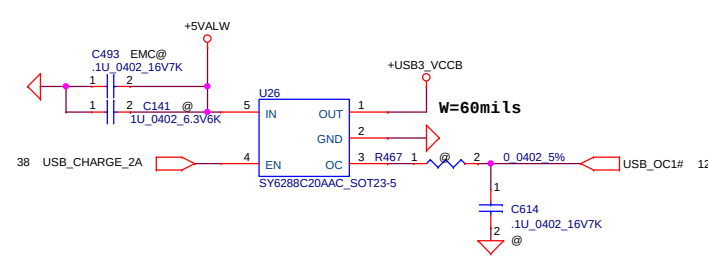
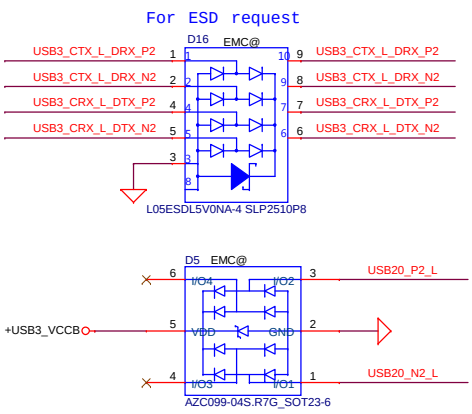
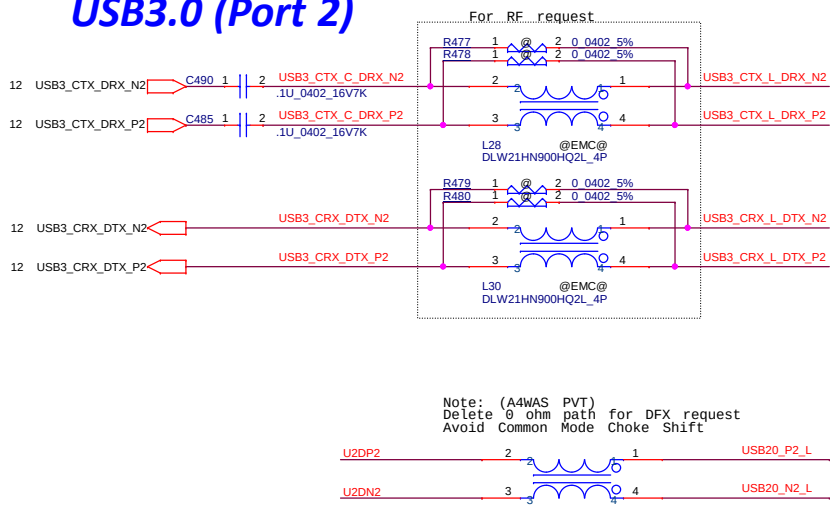


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								HDD/ODD/ HDD Re-Driver			
Size		Document Number						A4WAS M/B LA-C611P		Rev 1.0	
Date:		Tuesday, June 16, 2015		Sheet		36		of		60	

USB3.0 (Port 1)

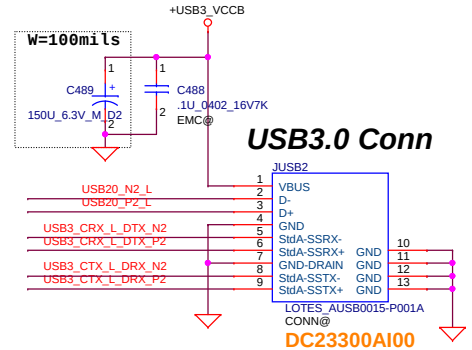
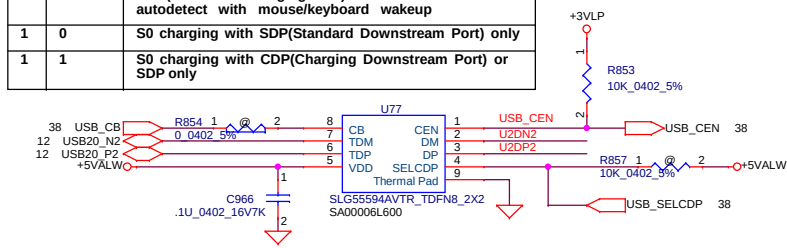


USB3.0 (Port 2)

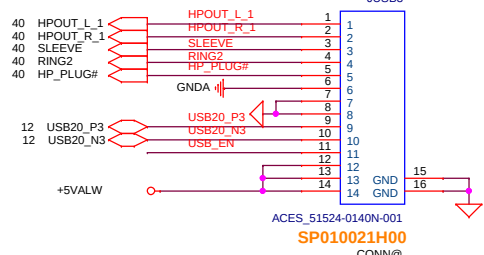


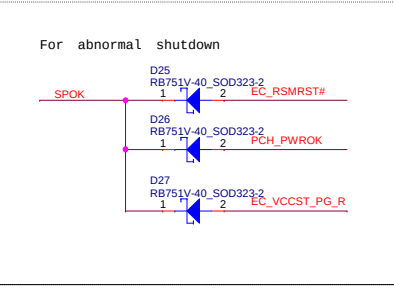
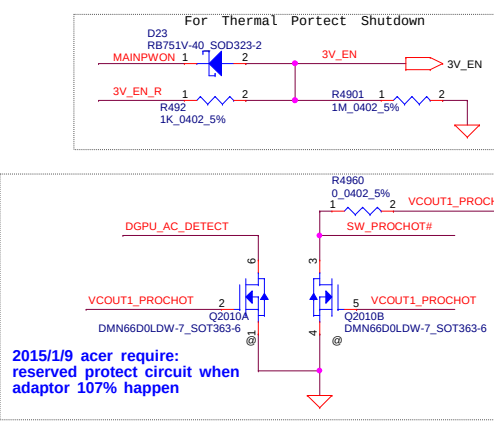
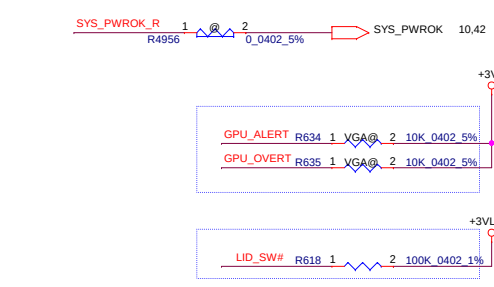
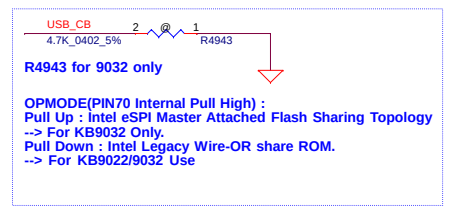
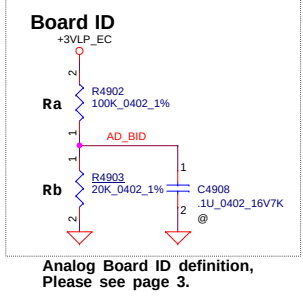
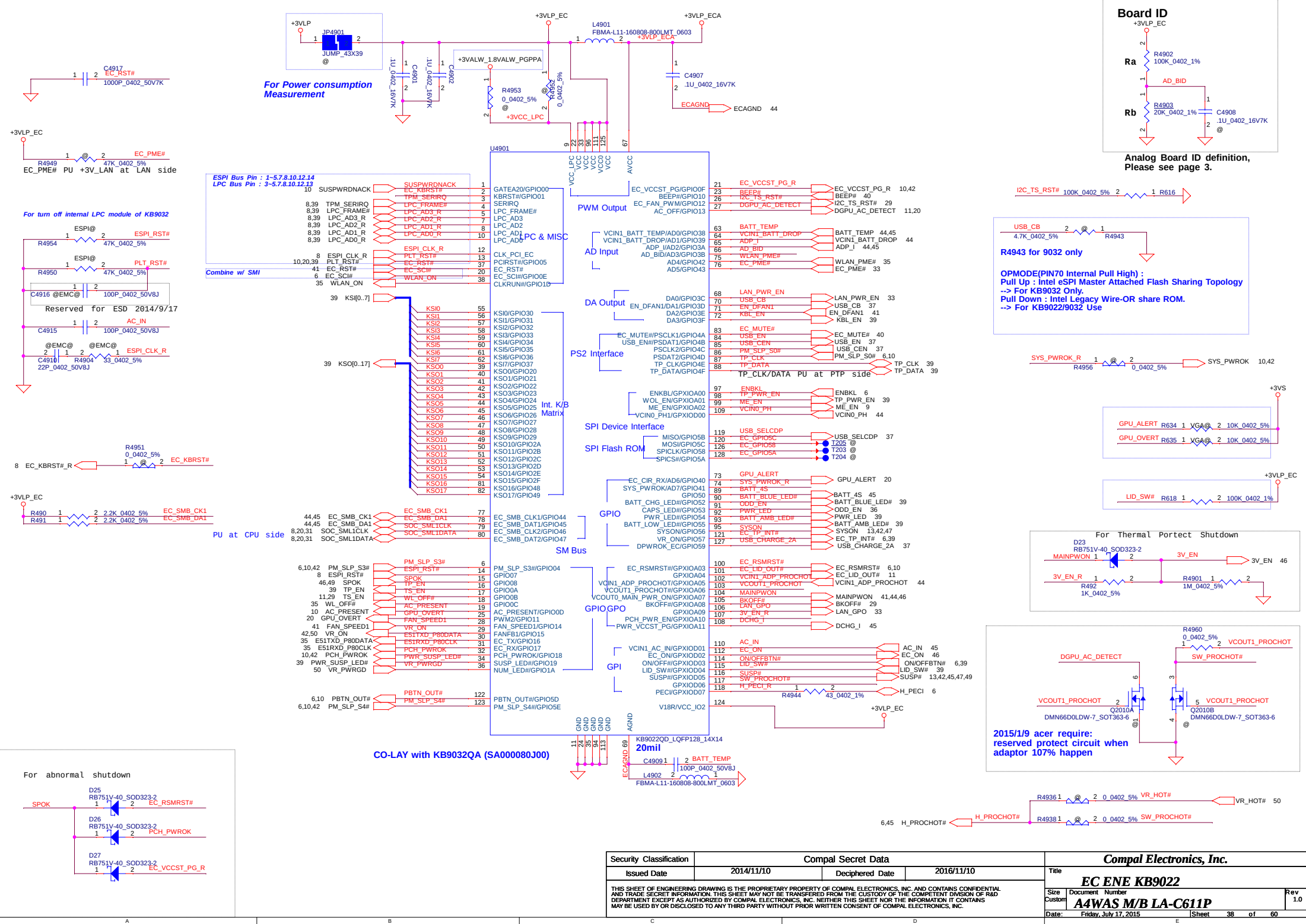
USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autotetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

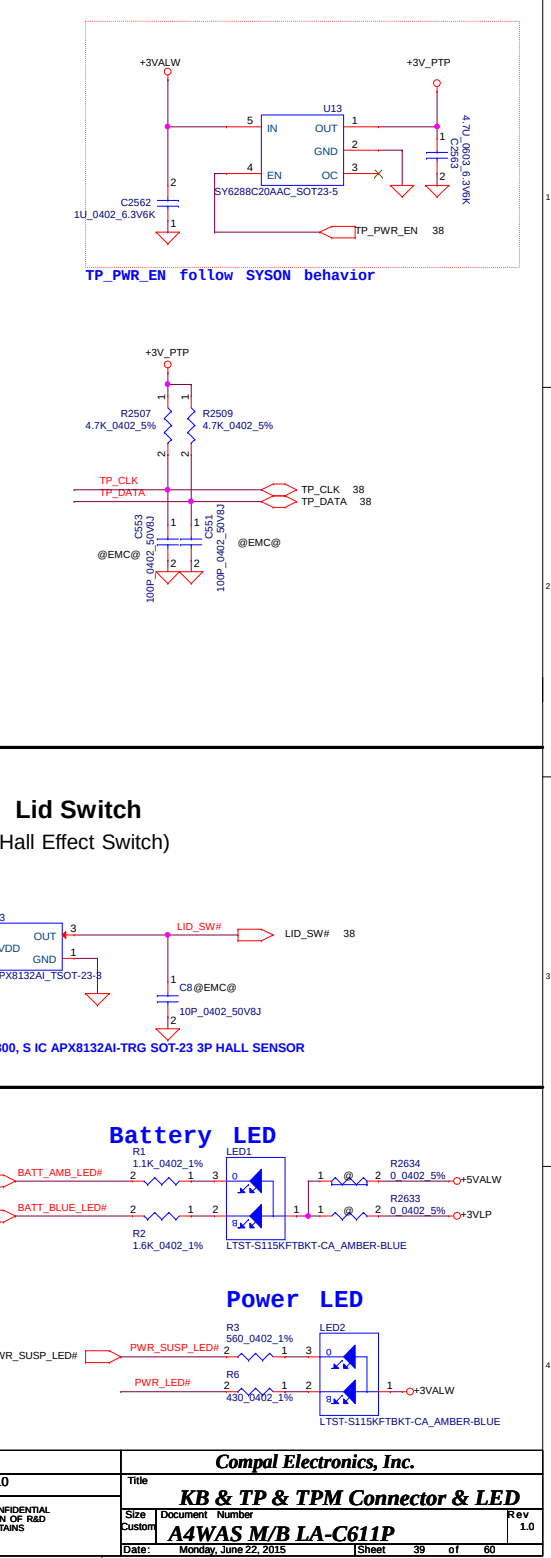
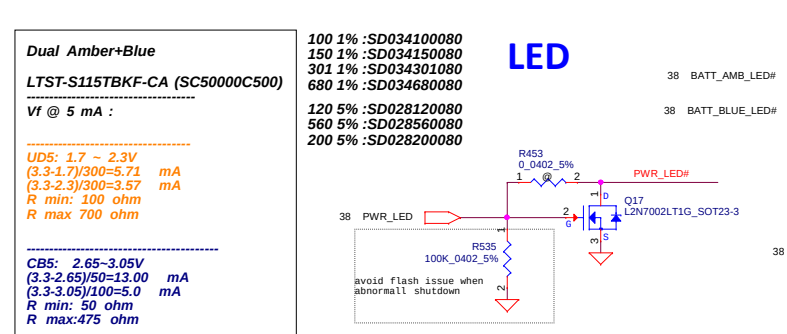
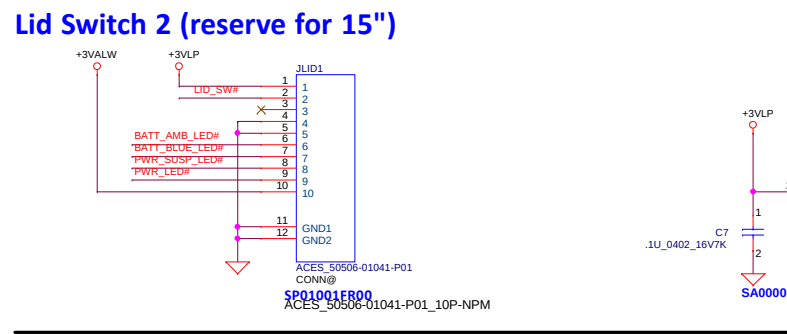
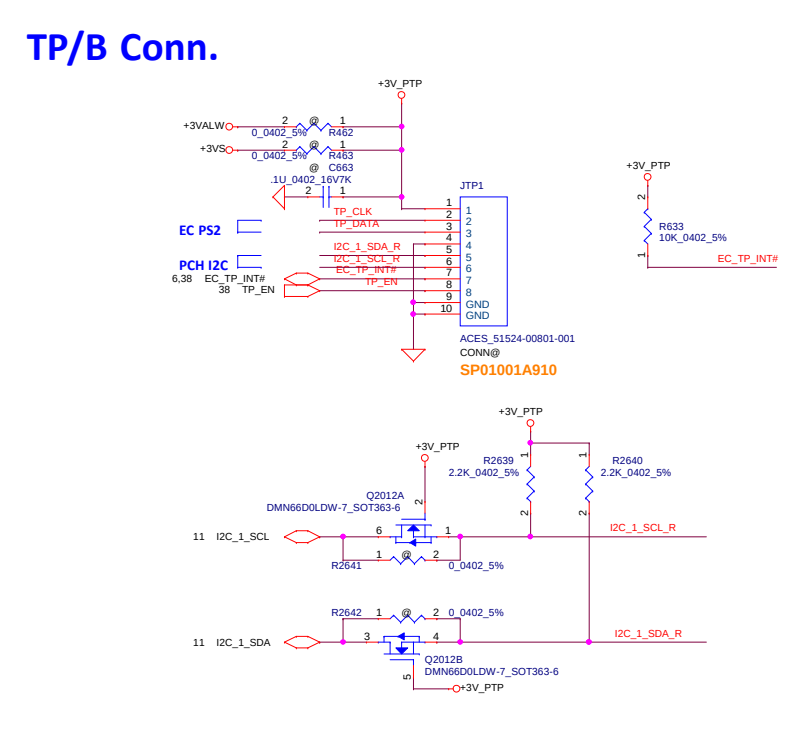
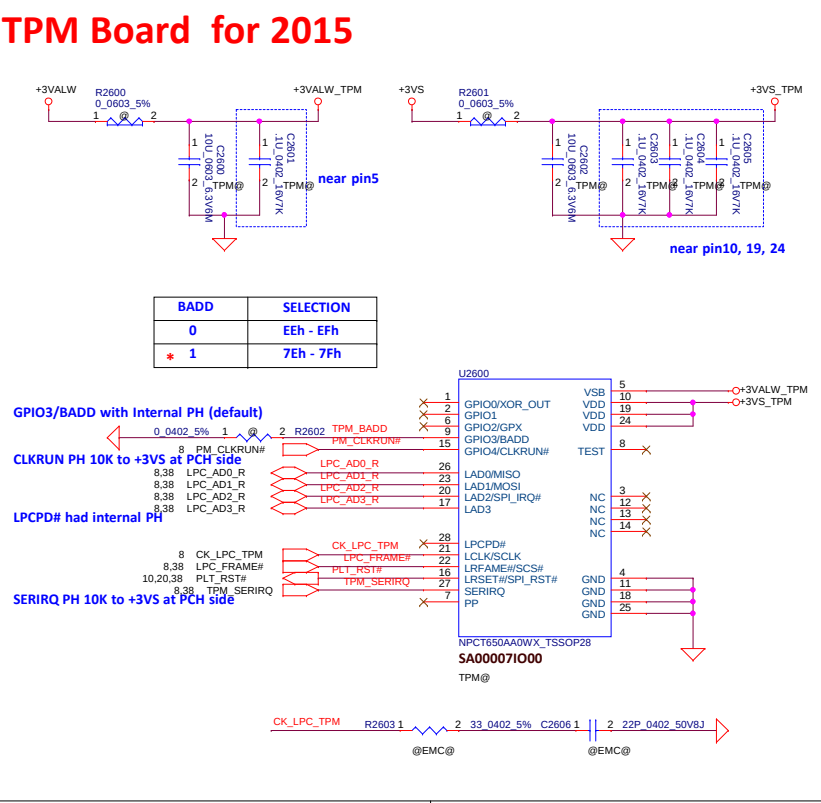
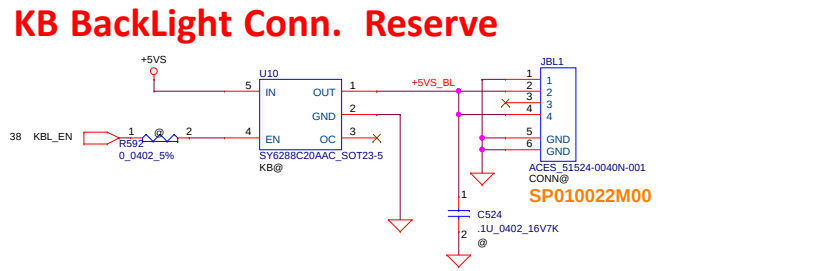
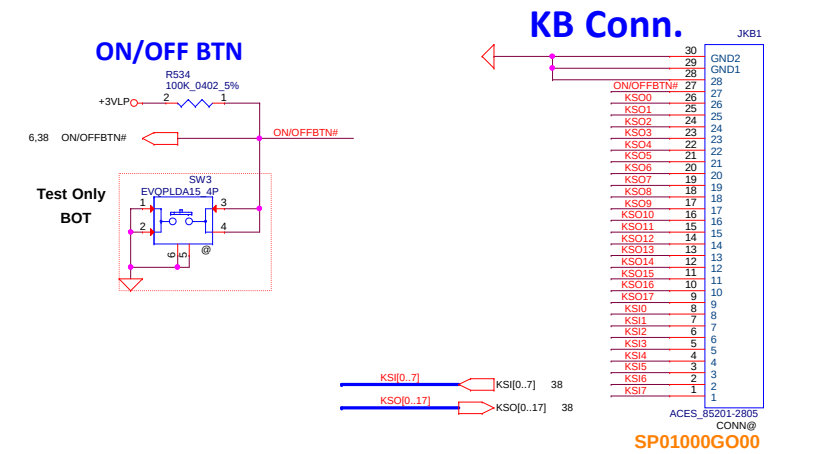


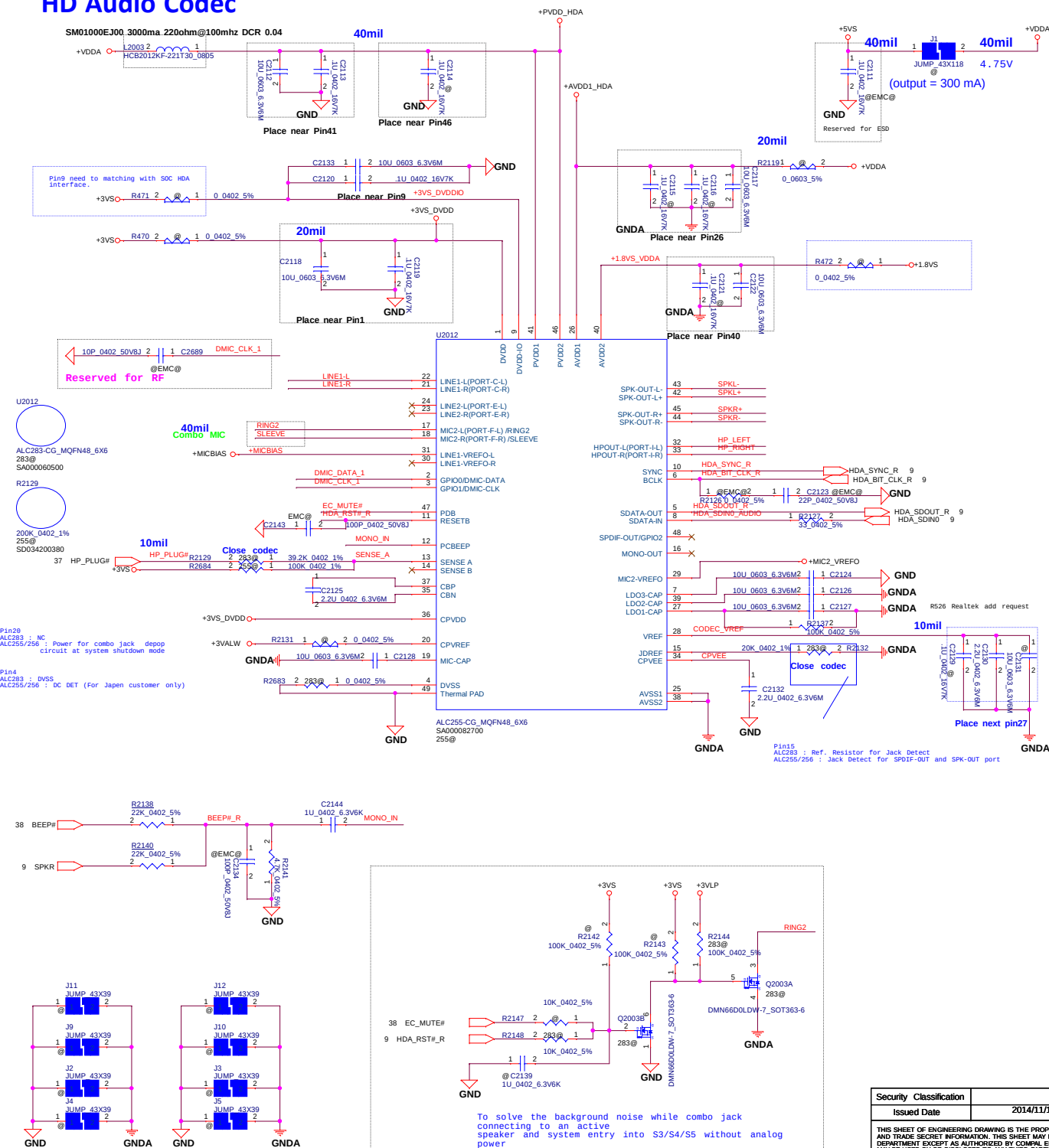
USB/B (USB Port 3, + AUDIO)



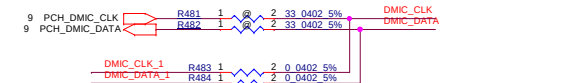
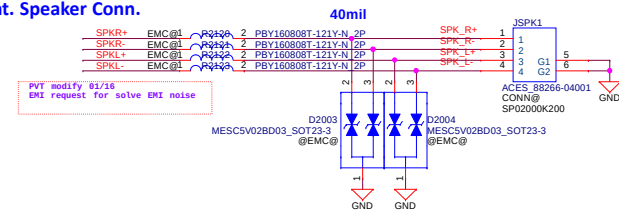


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								Document Number		1.0	
								A4WAS M/B LA-C611P			
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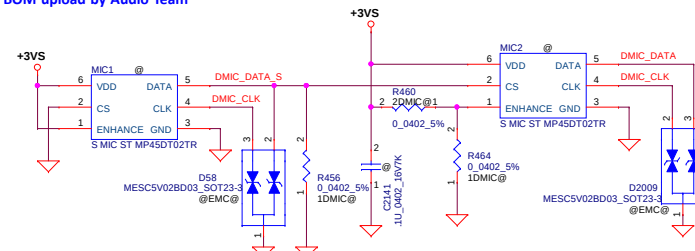


Int. Speaker Conn.

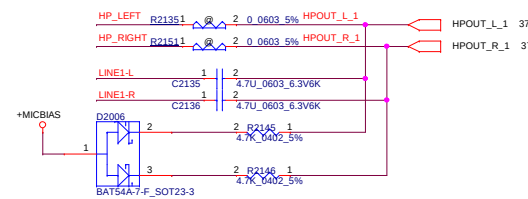
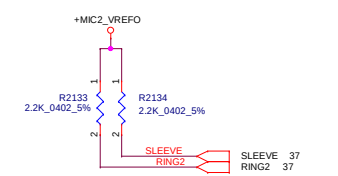


Digital MIC Dual-MIC

MIC BOM upload by Audio Team

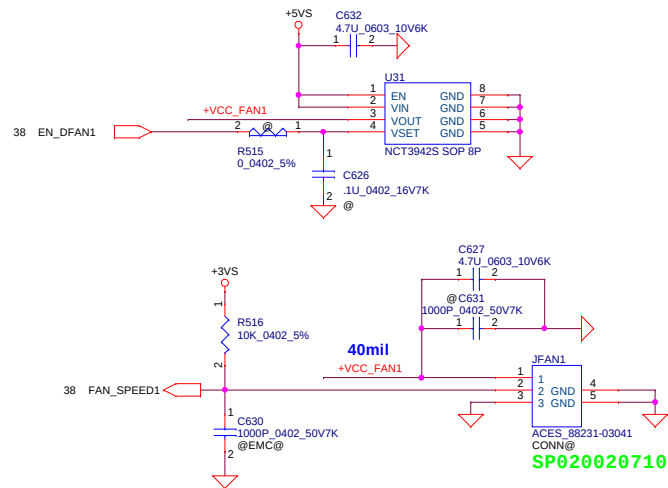


Headphone Out

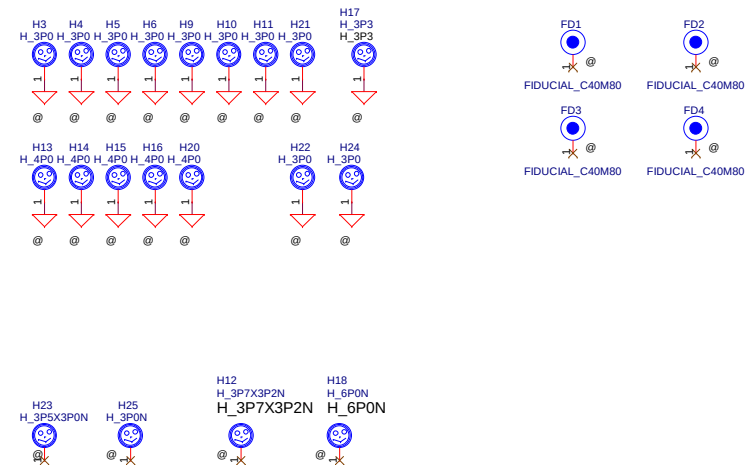


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				A4WAS M/B LA-C611P	
				Date	Tuesday, June 16, 2015
				Sheet	an of an

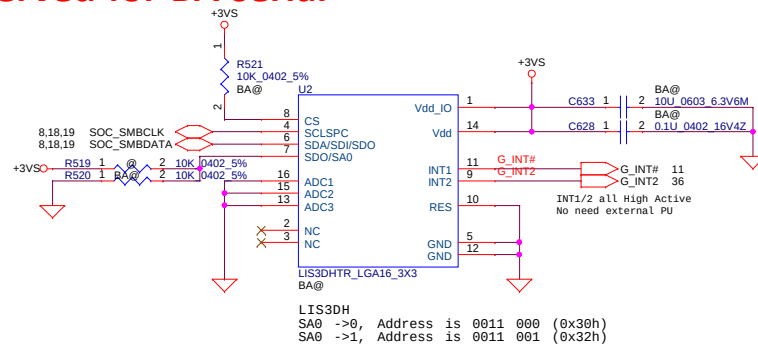
FAN1 Conn



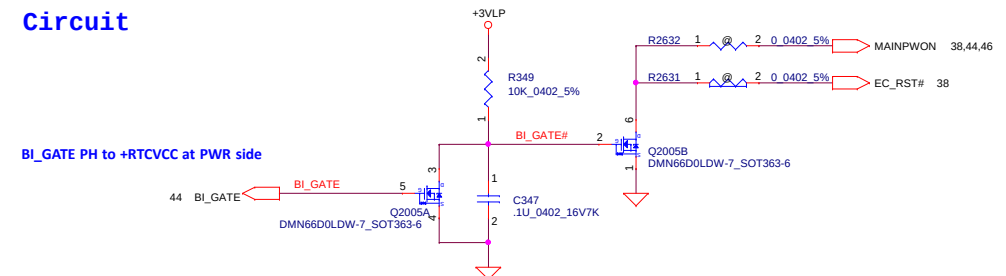
Screw Hole



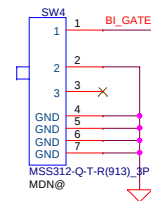
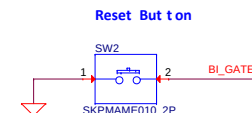
G-Sensor reserved for BA serial



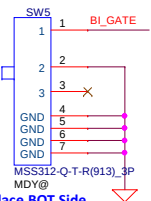
Reset Circuit



Debug SW



1-2 : Battery Off
2-3 : Battery ON

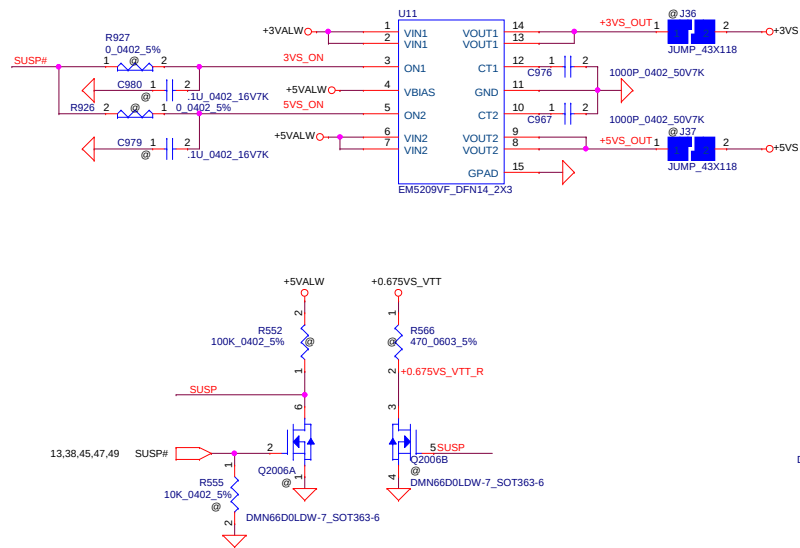


Place BOT Side 

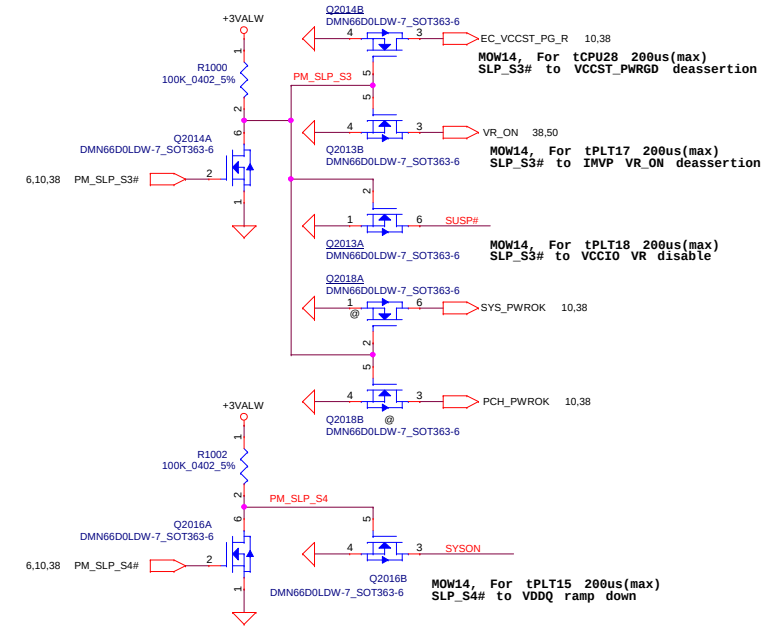
Reserved for memory door only

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				Size	Document Number
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				Date:	Thursday, July 16, 2015
				Sheet	41 of 60

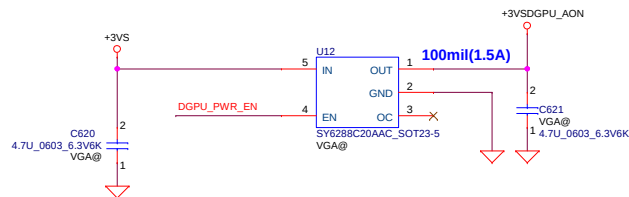
DC & VGA Interface



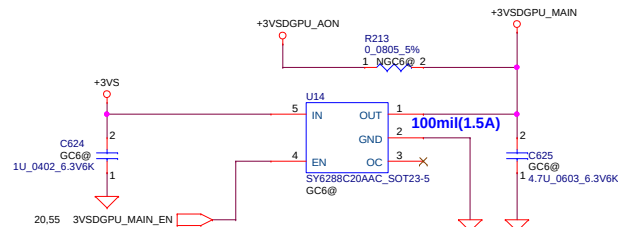
For Power ON/Off Sequence



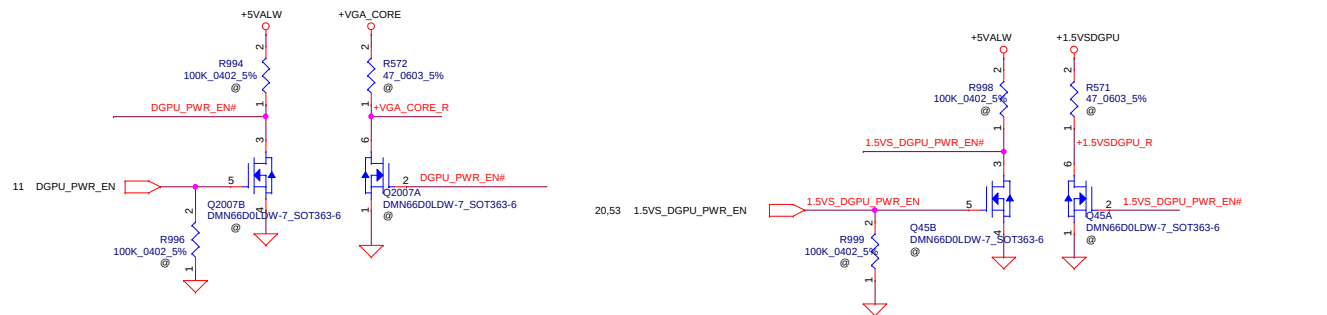
+3VS to +3VSDGPU_AON for GPU



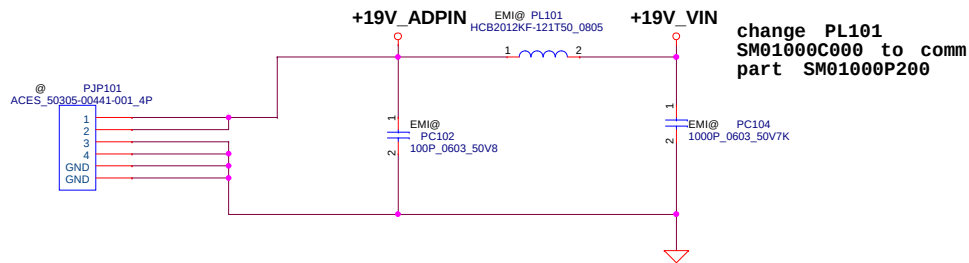
+3VS to +3VSDGPU_MAIN for GC6-2.0



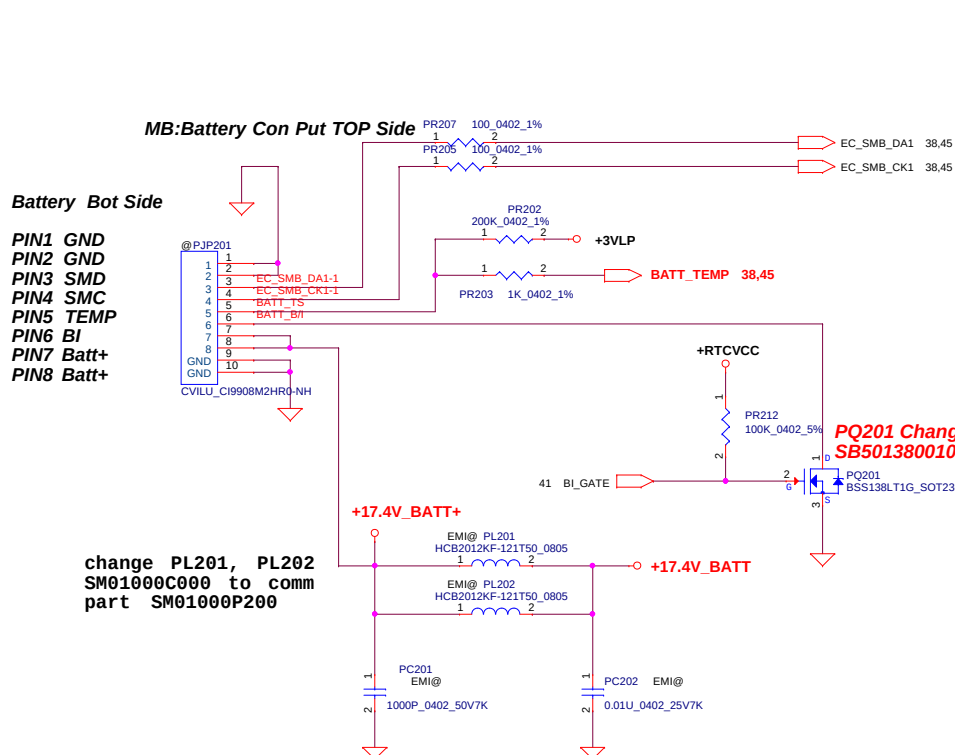
3VSDGPU_MAIN_EN From GPU



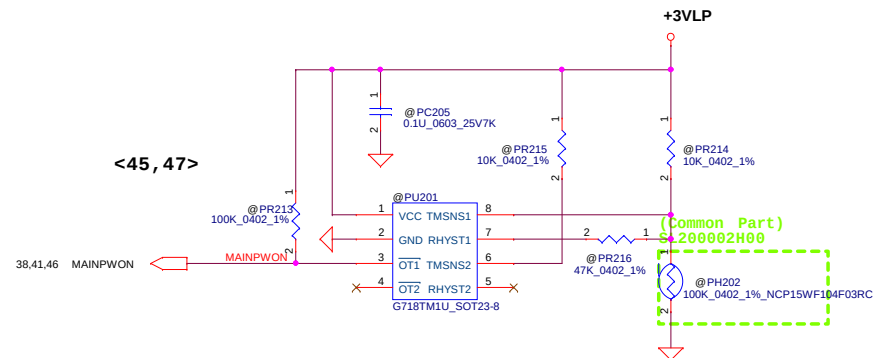
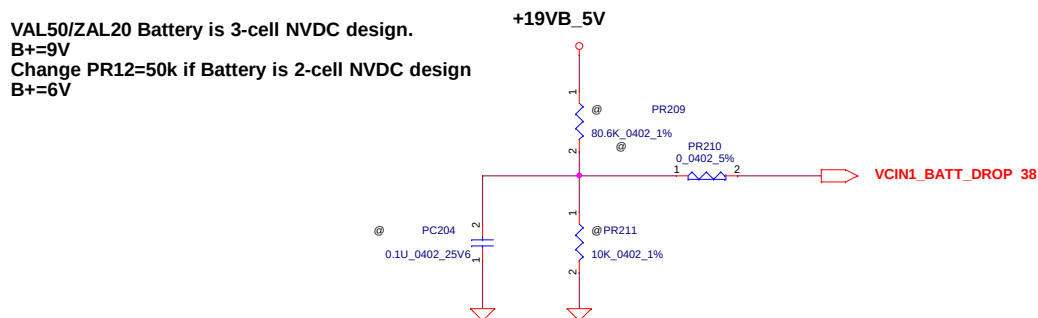
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Issued Date	2014/11/10	Deciphered Date	2016/11/10	Title	DC Interface	
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				Date:	Tuesday, June 16, 2015	Sheet 42 of 60



2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



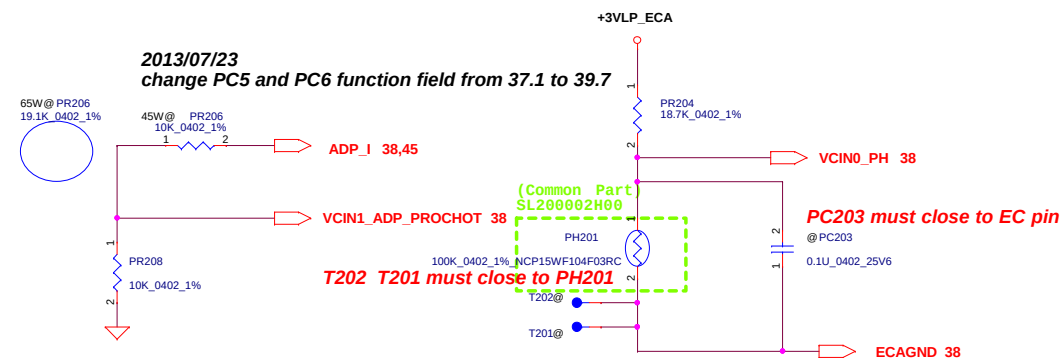
2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.



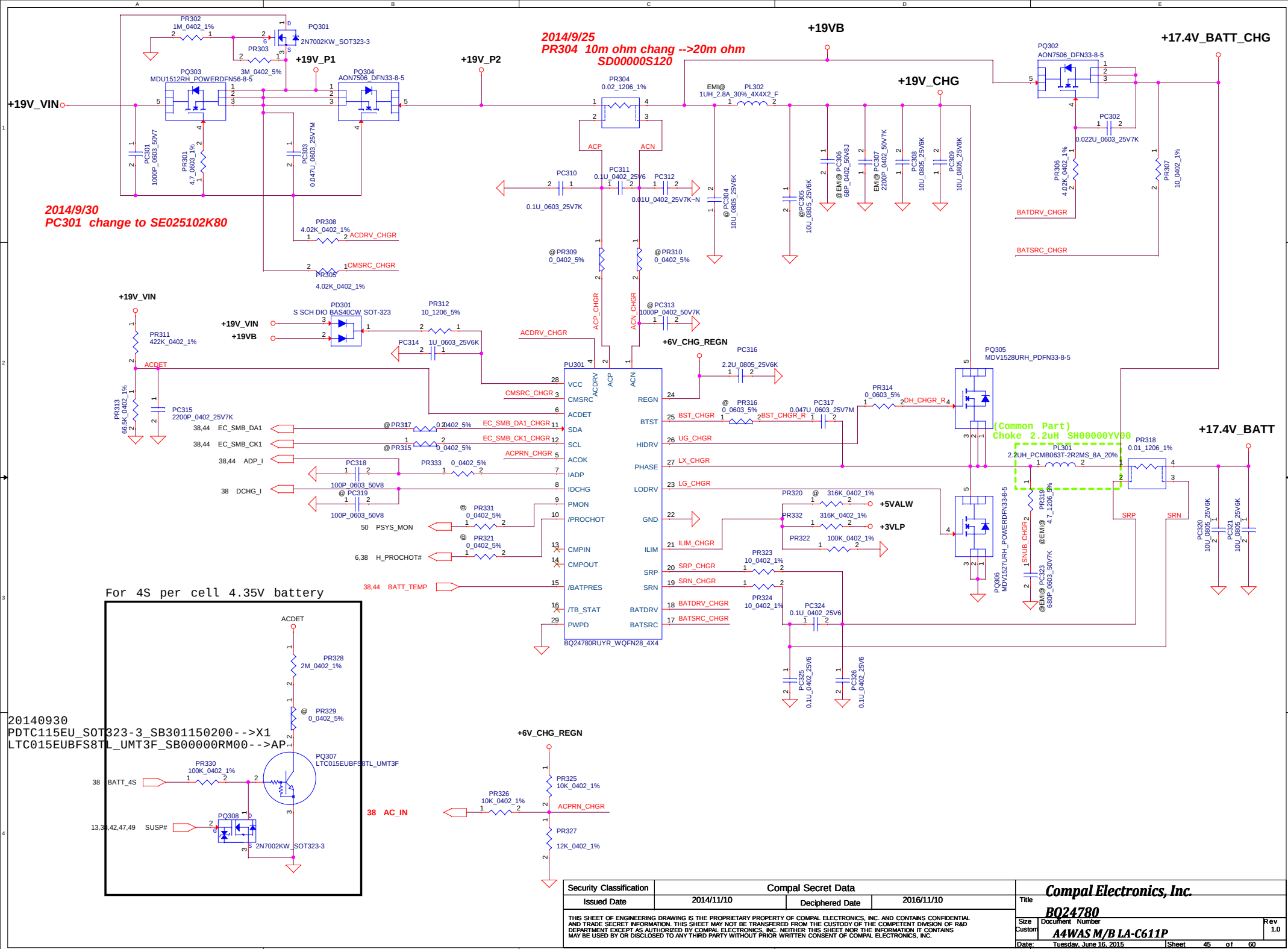
2014/09/25 update

For KB9022 sense 20mΩ	Active	Recovery
45W PR206 10K ohm SD034100280	58.5W, 0.61V	45W, 0.47V
65W PR206 19.1K ohm SD034191280	84.5W, 0.61V	65W, 0.47V

PH1 under CPU botten side :
CPU thermal protection at 89 +3 degree C
Recovery at 56 +3 degree C

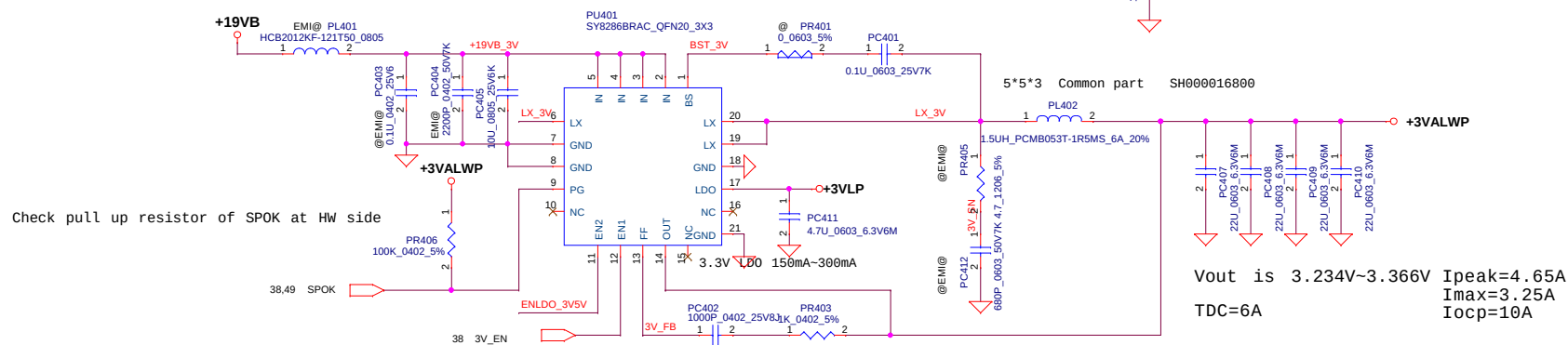


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				Custom	1.0
				A4WAS M/B LA-C611P Date: Monday, June 22, 2015	Sheet 44 of 60

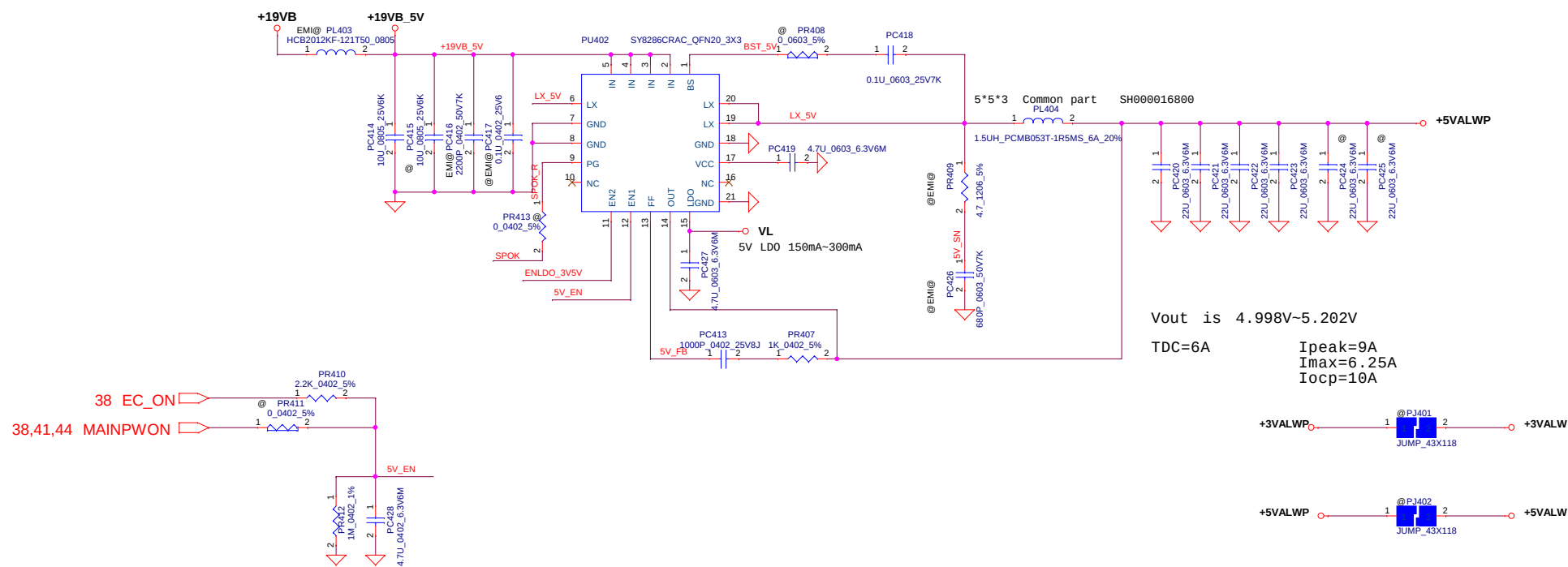


TPS51225C_V1.mdd

EN1 and EN2 dont't floating



Vout is 3.234V~3.366V Ipeak=4.65A
Imax=3.25A
TDC=6A Iocp=10A



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				Date:	Tuesday, June 16, 2015	Sheet 46 of 60

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

EMI@ PL501
HCB2012KF-121T50_0805

+19VB_CPU



```
change PL501
SM01000C000 to comm
part SM01000P200
```

Choke 1.5uH SH000016700
Common Part 7*7*3

Update Pc510 change
to Common Part
SF000006S00 20141227

change PQ502 form
to 7716, 20150108

453Kohm - ->455KHz

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
I_{peak}=10A

Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V
MOSFET footprint: SIS412DN

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

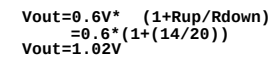
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

$$\begin{aligned} V_{out} &= 0.75V * \left(\frac{1 + R_{up}}{R_{down}} \right) \\ &= 0.75V * \left(1 + \left(\frac{8.06}{10} \right) \right) \\ &= 1.354V \quad 0.2\% \\ V_{out} &= 0.75V * \left(\frac{1 + R_{up}}{R_{down}} \right) \\ &= 0.75V * \left(1 + \left(\frac{8.2}{10} \right) \right) \\ &= 1.365V \quad 1.1\% \end{aligned}$$

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SYX196D_V3.mdd

+19VB_1VALW

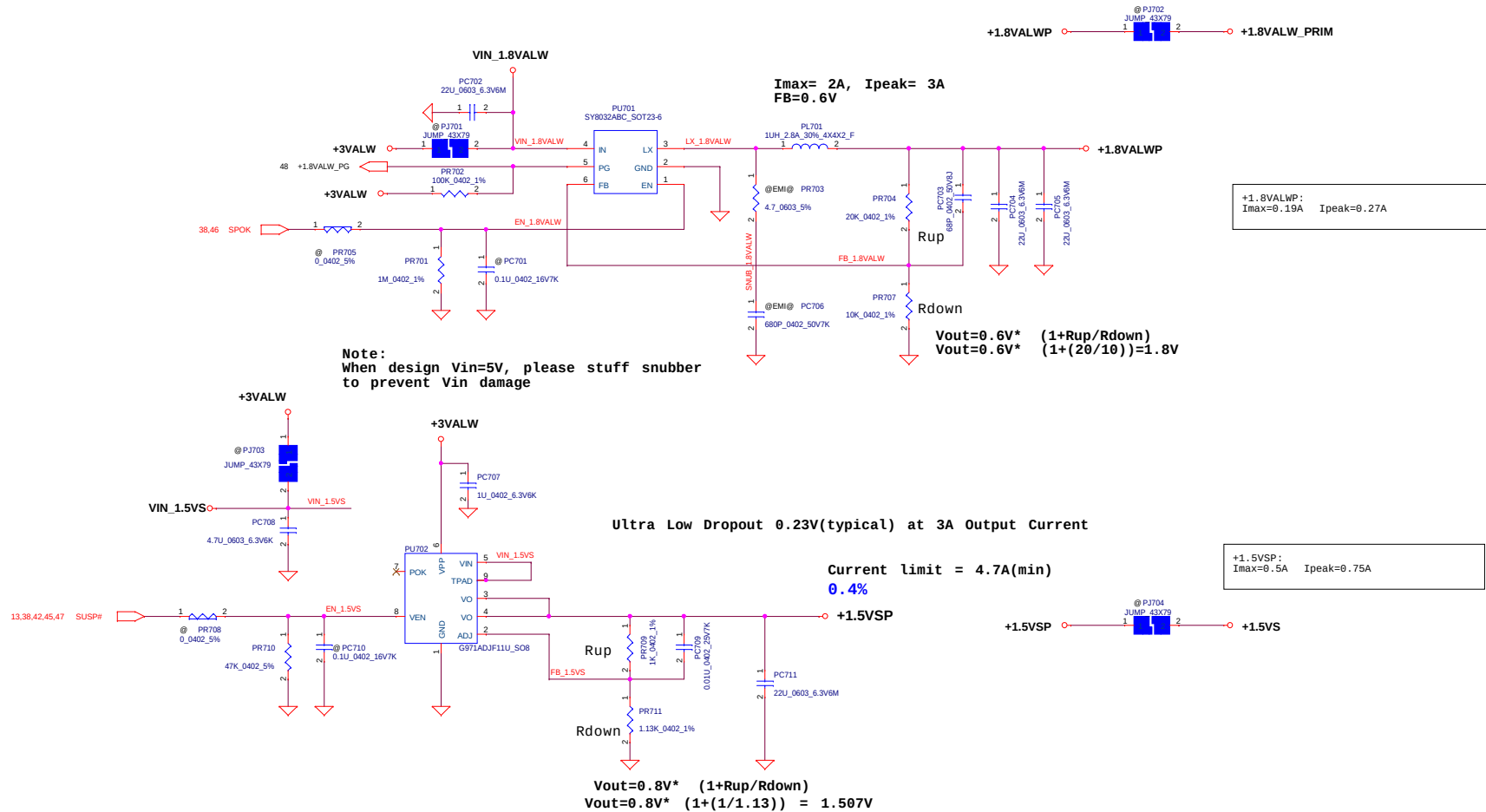


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Function Field :
VCCEDPIO  : IC-35.21 , others - 35.22
VCCEDRAM  : IC-35.25 , others - 35.26
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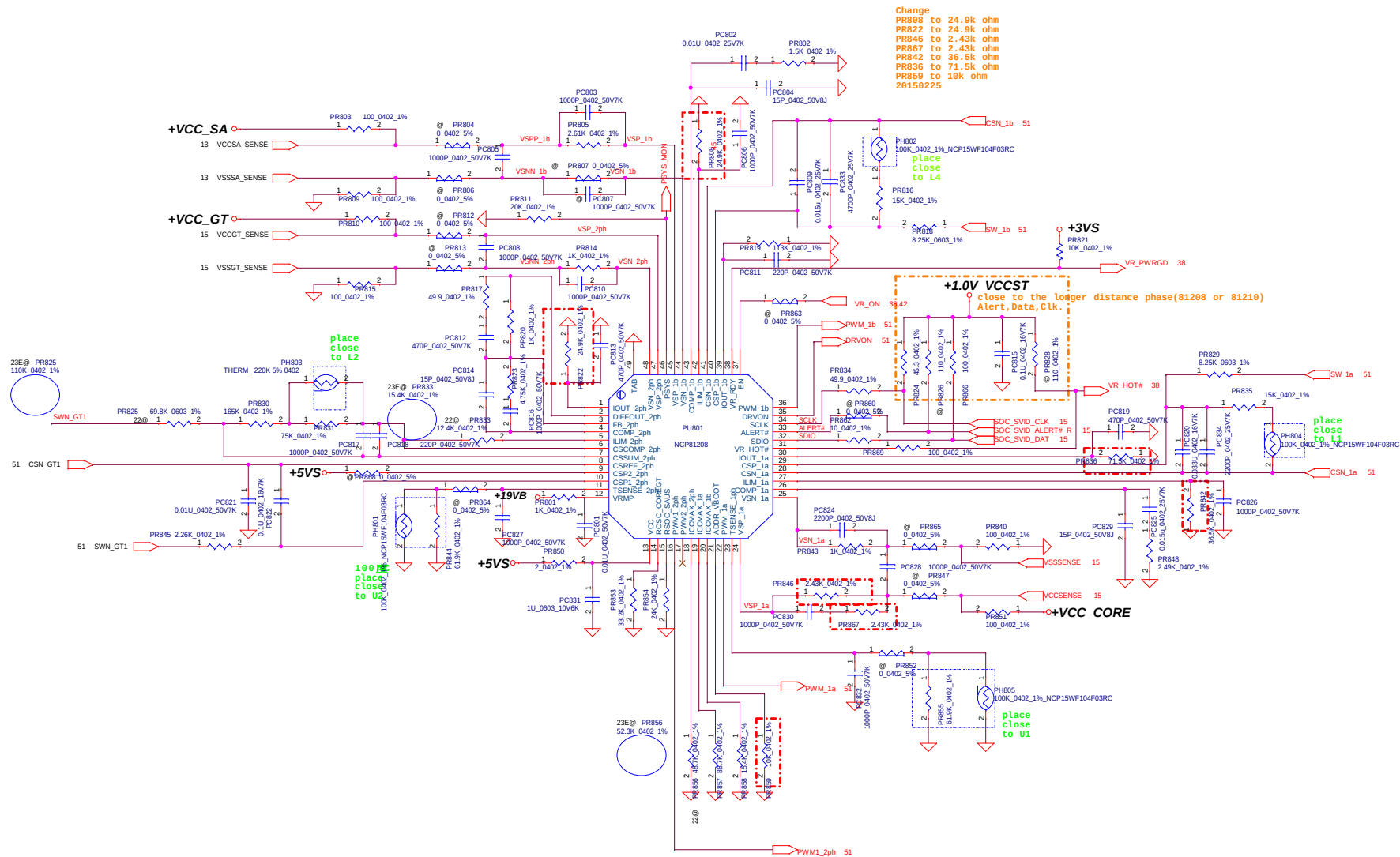
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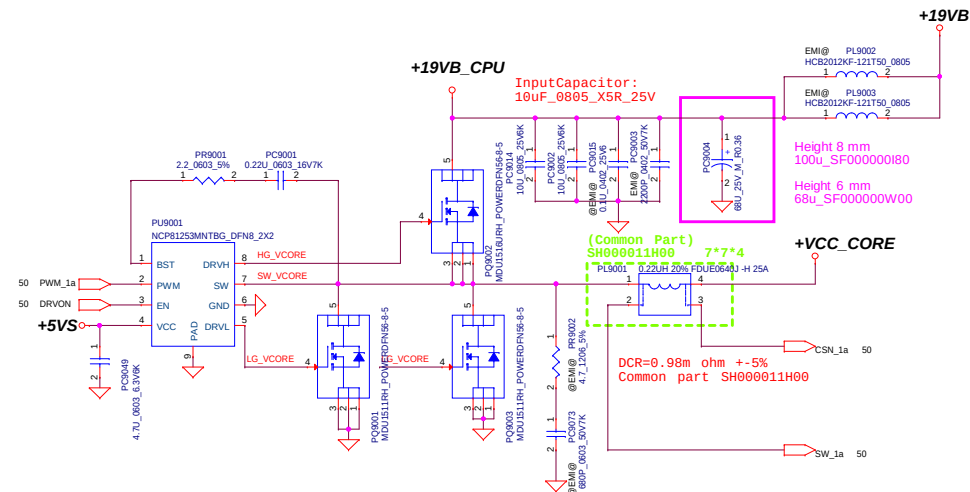
Module model information

SY8032_V2.mdd

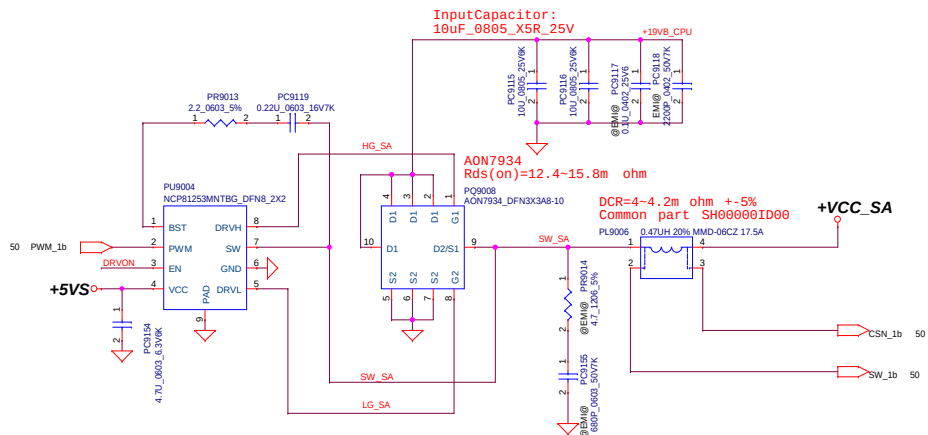
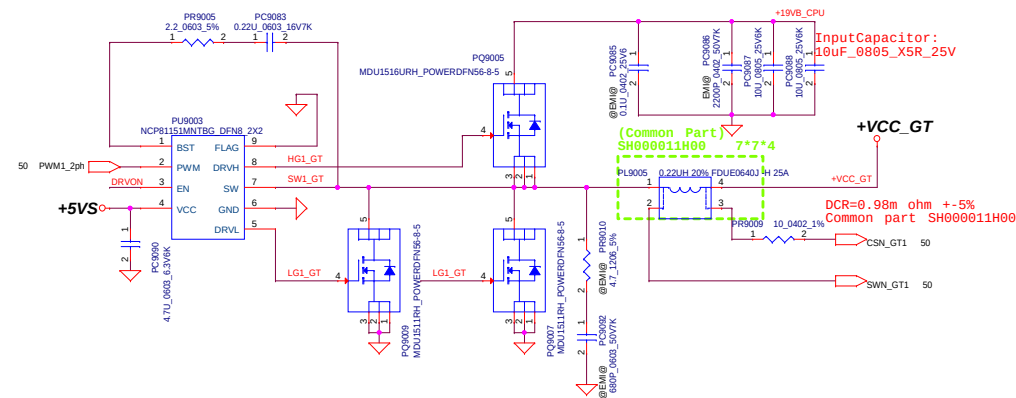


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				Size
				Document Number
				A4WAS M/B LA-C611P
				Rev
				1.0
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				Sheet 49 of 60





VCC:	Imax=19.6A	Ipeak=28A	Iocp=34A
VCCGT:	Imax=25.9A	Ipeak=37A	Iocp=44A
VCCSA:	Imax=4.5A	Ipeak=3.15A	Iocp=5.4A



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(Common Part)
SGA00009S00

(Common Part)
SGA00009S00

1uF_0201 SE000000U200 ,
SE000000UC00 .

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2014/11/10		2016/11/10		Power Train	
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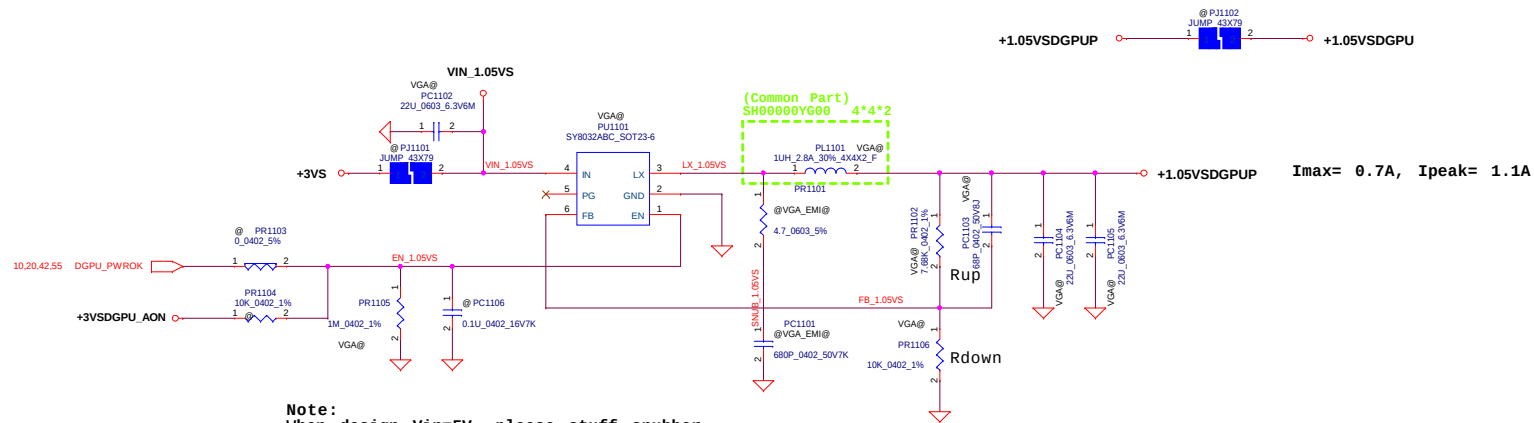


VFB=0.6V
 $V_{out}=0.6V \cdot (1+R_{up}/R_{down})$
 $V_{out}=1.365V$

Vout=0.6V* (1+(25.5/20))=1.356
 Vout=0.6V* (1+(30.9/20))=1.527

Module model information

SY8032_V2.mdd



Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

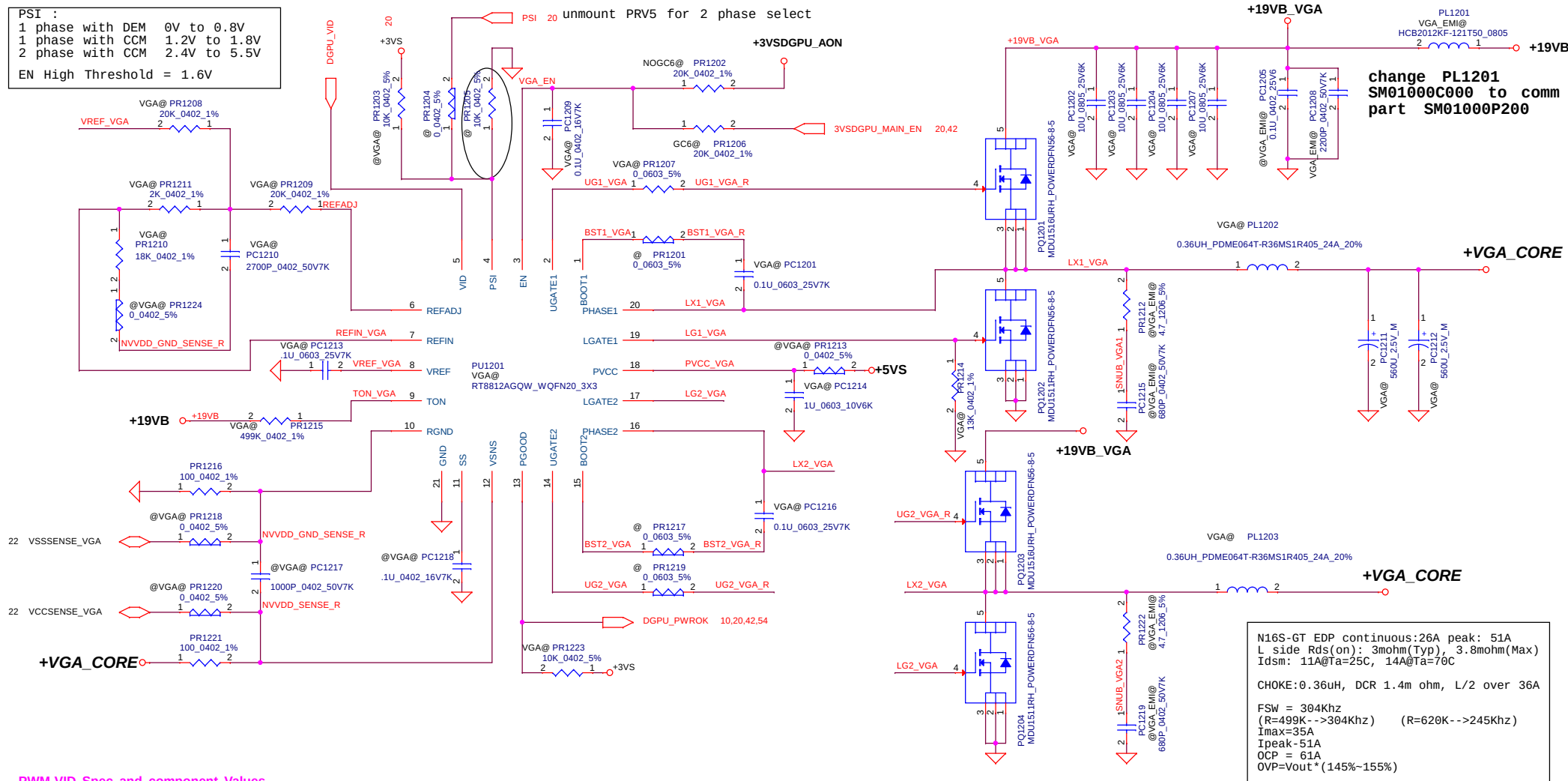
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

$$\Rightarrow 0.6V * (1 + (7.68/10)) = 1.061 \quad (1.01\%)$$

$$\Rightarrow 0.6V * (1 + (7.87/10)) = 1.072 \quad (2.1\%)$$

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PSI :
 1 phase with DEM 0V to 0.8V
 1 phase with CCM 1.2V to 1.8V
 2 phase with CCM 2.4V to 5.5V
 EN High Threshold = 1.6V

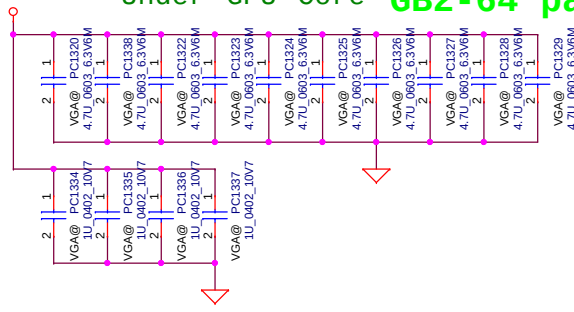


PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR	20K	39K	27K
Rref1	PR	20K	30K	7.5K
Rboot	PR	2K	3K	0
Rref2=PR1209	PR	18K	24K	6.2K
+PR1212	PR	0	3K	1.74K
C	PC	2.7nf	1.8nf	5.6nf

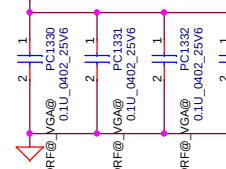
N16S-GT
 N16V-GM

+VGA_CORE Under GPU Core GB2-64 package

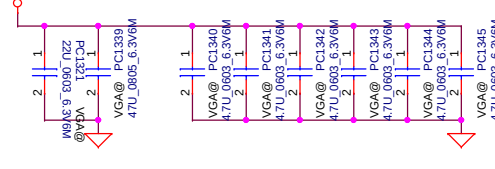


Remove GPU OTP circuit for HW request

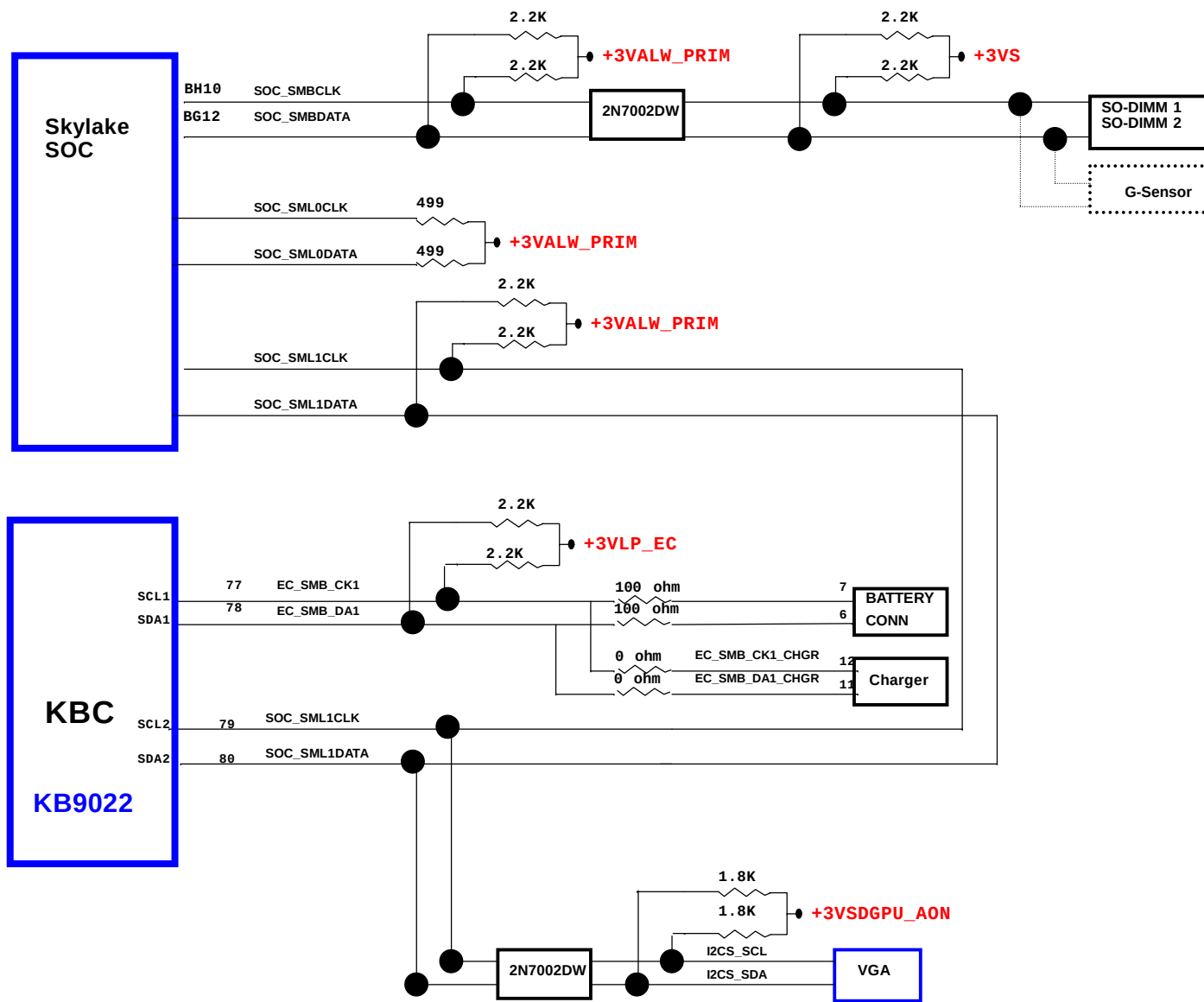
+VGA_CORE



+VGA_CORE Near GPU Core



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2014/11/10		2016/11/10		SMBUS Routing Table	
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Change.	change to the latest 2015 for MOSFET application.	01	45	change PQ305 to MDV1528 & PQ306 MDV1527		EVT
02	Design Change.	change to the latest 2015 for MOSFET application.	01	47	change PQ503 to MDV1528		EVT
03	Design Change.	change to the latest 2015 for MOSFET application.	01	51	change PQ9002 & PQ9005 to MDU1516		EVT
04	Design Change.	change to the latest 2015 for MOSFET application.	01	51	change PQ9001, PQ9003, PQ9007 & PQ9009 to MDV1511		EVT
05	Design Change.	change to the latest 2015 for MOSFET application.	01	57	change PQ1201 & PQ1203 to MDU1516		EVT
06	Design Change.	change to the latest 2015 for MOSFET application.	01	57	change PQ1202 & PQ1204 to MDU1511		EVT
07	power off pulse issue when S0 → S5.	+0.675VS have a pulse when S0→S5 as attached.	01	47	change Pu501 8207P to 8207M		EVT
08	power off pulse issue when S0 → S5.	8207M output cap is use 330uF poscap	01	47	Delete PC510~PC515 22u*6		EVT
09	power off pulse issue when S0 → S5.	8207M output cap is use 330uF poscap	01	47	Add PC510 330u*1		EVT
10	power off pulse issue when S0 → S5.	8207M frequency is different with 8207P	02	47	change PR507 to 887k ohm		DVT
11	Design Change.	Tune +1.5VSDGPUP enable time	02	53	change PR1002 to 40.2k ohm		DVT
12	Stop use Anpec LDO	Anpec LDO is EOL	02	49	change Pu702 to G971		DVT
13	DFB request	pin is too small, avoid open solder	02	44	Change PJP201 SP021210250 (ACES_50458-00801-001_8P-T) to SP020017H00 (CVILU_CI9908M2HRO-NH_8P)		DVT
14	Tune CPU transient	Tune CPU transient	02	50	Change PR808 to 24.9k ohm PR822 to 24.9k ohm PR846 to 2.4k ohm PR867 to 2.4k ohm PR842 to 36.5k ohm PR836 to 69.8k ohm PR859 to 10k ohm		DVT
15	Design Change.		02	45	Change PC315 0.1u to 2200p		DVT
16	Design Change.	change 1V output from 1.011V to 1.02V	02	48	Change PR608 13.7k to 14k ohm		DVT
17	Tune CPU transient	Tune CPU transient	02	50	Change PR846 to 2.43k ohm PR867 to 2.43k ohm PR836 to 71.5k ohm		DVT
18	Design Change	Change to common part	02	53	Change PL9002, PL9003, PL1001 & PL1201 to common part (HCB2012KF-121T50_0805)		DVT
19	thermal request	change PH1 from 92degree to 89degree	02	44	Change PR204 from 16.9k ohm to 18.7k ohm		

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1	11	CPU	1/9	NA	Reserved RC189(0 ohm) for DGPU_AC_DETECT	DVT	0.2
2	38	EC	1/9	Reserved protect circuit when adaptor 107% happen, requirer from Acer	Change net from VCOUT1_PROCHOT# to VCOUT1_PROCHOT Change U4901.117 from SEN_DET# to SW_PROCHOT# Reserved Q2010A/B for SW_PROCHOT# and DGPU_AC_DETECT Add R4960 for SW_PROCHOT# and VCOUT1_PROCHOT Rename R4938.2 to SW_PROCHOT#	DVT	0.2
3	38	EC	1/9	Remove unuse part	Delete R4905, R619, R4958	DVT	0.2
4	10	CPU	1/12	SYS_RESET# Pull-up to ALWAYS power rails	Change RPC11.6 to +3VALW_PRIM	DVT	0.2
5	11	CPU	1/12	Reserved PD for G_INT#	Reserved RC117 for G_INT#	DVT	0.2
6	11	CPU	1/12	NA	Move RC212 to Page06 and add note for EC_SCI#	DVT	0.2
7	11	CPU	1/12	Separate RPC18 for easy PU	Change RPC18 to RC126, RC127 (1K) and RC128, RC129 (2.2K)	DVT	0.2
8	17	CPU	1/12	Reserved for Cannonlake-U (2014MOW52)	Connect UC1.U11/U12 to +1.8VALW_PRIM and reserved CC79 for UC1.U11/U12	DVT	0.2
9	18, 19	Memory	1/12	Change CIS Symbol and Footprint	Change CD16,CD46 PN to SGA00009S00	DVT	0.2
10	29, 37	USB	1/12	Change CIS Symbol and Footprint	Change L24,L25,L26,L28,L29,L30, L27 CIS Symbol to SM070003Y00	DVT	0.2
11	33	LAN	1/12	Reserved path for +3V_LAN	Reserved R214 0_0850 for +3V_LAN	DVT	0.2
12	35	WLAN	1/12	Disconnect SUSCK to M.2 connector to avoid leakage current	R426 change to 0_0402 @	DVT	0.2
13	37, 38	USB	1/12	Control USB Charger behavior when disabel USB charger funct i on	Change R854.1 from SUSP# to USB_CB and U4901.70 from OPMODE to USB_CB	DVT	0.2
14	38	EC	1/12	Board ID change to DVT	Change R4903 from 0_0402_5% to 12K_0402_5%	DVT	0.2
15	38	EC	1/12	Remove unuse part	Delete R4957, R4959	DVT	0.2
16	39	LED	1/12	LED light adjust	Change R3 to 560 ohm and change R6 to 430 ohm Change R2633.2 to +3VLP	DVT	0.2
17	39	LID	1/12	Change Hall Sensor IC	Change U3 to SA00008K800 (ANPEC)	DVT	0.2
18	39	PTP	1/12	Add level shift for PTP I2C interface	Add Q2012A/B, R2641, R2642, R2639, R2640 Change RC128,RC129 PU to +3VALW_PGPPC	DVT	0.2
19	41	Others	1/12	Follow DFX requirerment	Change H17 from 3P2 to 3P3	DVT	0.2
20	42	Sequence	1/12	For power off sequence	Add R1000, R1002, Q2013, Q2014, Q2016 for tCPU17, tCPU18, tCPU28, tPLT15	DVT	0.2
21	06	Debug	1/15	Reserved for power on select	Reserved RC53, RC54 for JAPS1.11	DVT	0.2
22	36	HDD	1/15	Pin def i rit on modfy	JHDD2.10 connect to GND	DVT	0.2
23	39	Others	1/15	Pin def i rit on modfy	JLID1.2 change to LID_SW#, JLID1.3 NC	DVT	0.2
24	08	SPI	1/20	Remove/Un-Pop unuse part	Del RC203 and change un-pop RPC6	DVT	0.2
25	09, 40	DMIC	1/20	Reserved DMIC path from SOC	Reserved R481, R482 for PCH_DMIC_CLK/DATA from UC1.H5/D7 Add R483, R484 0_0402 for Audio DMIC	DVT	0.2
26	22	NV	1/20	Update HYNIX C die straps table	Update HYNIX C die straps table	DVT	0.2
27	30	Others	1/20	Remove unuse part	Del R377, R378, R376	DVT	0.2
28	35	WLAN	1/20	Separate M.2 pin32 and 46 for Intel WLAN 3165	JNGFF1.32 change to NC (for Intel 3165)	DVT	0.2
29	38	Sequence	1/20	For power down sequence	Add D27 for EC_VCCST_PG_R	DVT	0.2
30	39	LED	1/20	Update CIS Symbol and Footprint	Update LED1, LED2 CIS Symbol	DVT	0.2
31	40	Audio	1/20	Update BOM Structure	Change R2135, R2151 to EMC@	DVT	0.2
32	40	Audio	1/20	Adjust MONO_IN input voltage	Change R2140 to 27K and R2138 to 27K(@)	DVT	0.2
33	41	Others	1/20	Change reset signal	Mount R2631 and un-mount R2632	DVT	0.2
34		Others	1/20	Change 0 ohm to R-Short	0_0603 to R-Short: R2075, R81, RC176, RC209 0_0402 to R-Short: R2131, RC172, R472, R927, R2552, R4953, R4956, RC178, RC197, R427,R428	DVT	0.2
35	20	NV	1/28	Remove unuse part	Del D2002, R2055	DVT	0.2
36	30	HDMI	1/28	Remove unuse part	DEL ZZZ1 (HDMI ROYALTY)	DVT	0.2
37	30	HDMI	1/28	Change U52 main source (HDMI power switch)	U52 change to SA00004ZA00	DVT	0.2
38	38	EC	1/28	Un-use part change to @	R4943 change to @	DVT	0.2
40	06	CMC	2/4	Change XDP to CMC	Change JXDP1 CIS symbol to CMC CIS Symbol(JPCMC1) Del RPC3, RC22, RC25, RC20, RC14, CC120, CC121, RPC4 Rerouting RPC2, RPC4, RPC15, RC23, RC151 Add RC17, RC55, RC56 Change RC37 to @ Change XDP@ to CMC@	DVT	0.2
41	08	LPC	2/4	Change 0 ohm to R-Short	Change RPC8 to RC144~ RC147 0 ohm R-short	DVT	0.2

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
42	10		2/4	Remove unuse part	Del RC108	DVT	0.2
43	10	SOC	2/4	Add T164/T165 for CLK_CPU_ITP/CLK_CPU_ITP#	Add T164/T165 for CLK_CPU_ITP/CLK_CPU_ITP#	DVT	0.2
44	10	SOC	2/4	Change Material of AND gate	Change UC3 to SA00000H00	DVT	0.2
45	12	SOC	2/4	Follow PCH EDS1.2 add PD resistor when un-use USB	Add RC130, RC131 for USB2_ID and USB2_VBUSSENSE	DVT	0.2
46	10	SOC	2/5	Reserved PD resistor (2014MOW48)	Reserved RC136 for Cannonlake-U	DVT	0.2
47	13	SOC	2/5	Reserved path for VCCIO	Reserved U4902, C977	DVT	0.2
48	06	SOC	2/9	Reserved path for TP_INT#	Reserved RC137	DVT	0.2
49	17	SOC	2/9	Reserved power source for U11/U12	Add RC57 for UC1.U11/U12	DVT	0.2
50	19	DIMM	2/9	Remove un-use part	Del CD46	DVT	0.2
51	29,37	USB Chock	2/9	Swap net because update CIS Symbol	SWAP net of L24,L25,L26,L28,L29,L30,L27	DVT	0.2
52	10	Crystal	2/11	Update 32.768KHz Crystal to 9pF	Change YC2 PN to SJ10000L000	DVT	0.2
53	41	D-Cover	2/25	Reserved SW5 for memory door on D-Cover	Reserved SW5(@)	DVT	0.2
54	14	PCH	2/26	Reserved for Intel PDG1.2 Table52-9	Reserved CC123, CC124,CC125	DVT	0.2
55	40	DMIC	3/2	Follow PDG1.2 Table28-3	R481,R482 change to 33 ohm	DVT	0.2
56	08	SPI	3/3	2015MOW06 no need PU1K on SPI_I02/I03	Un-Mount RC47	DVT	0.2
57	08	Crystal	3/3	Modify for 9pF Crysta	Change CC15,CC16 to 8.2pF	DVT	0.2
58	18,19	Memory	3/3	Mount decoupling capacitor	Mount and change CD1, CD17, CD28, CD47 to 0.1U 0402	DVT	0.2
59	35	SUSCLK	3/3	Del SUSCLK and reserved TP(Regruie from Acer)	Del R426, C85 and add T3806	DVT	0.2
60	39	Others	3/3	Un-mount un-use part	Un-mount SW3	DVT	0.2
61	08	SMBUS	3/3	Add level shift for SOC_SMBCLK/SOC_SMBDATA	change RC202, RC49, RC50, RPC7 PU to +3VALW_PRIM add Q2017, RC220, RC221, RC222, RC223 change net name from SOC_SMBCLK/SOC_SMBDATA to SOC_SMBCLK_1/SOC_SMBDATA_1	DVT	0.2
62	08	Others	4/1	Delete reserved component	change RPC7 PU to 2.2K Del RPC8, RC45, RPC6	PVT	0.3
63	08	SMBUS	4/1	Add BOM Structure for SPI ROM	Change RPC5 and RC52 to 15 ohm with 8M_SINGLE@ Add RPC5 and RC52 33 ohm with 8M_DUAL@ Add reserved component UC2 with 8M_DUAL@	PVT	0.3
64	08	SMBUS	4/1	Delete EC SPI path	Del RPC6	PVT	0.3
65	08	SPI	4/1	MOW36 QS sample no need to PD	Change RC51 to ES@	PVT	0.3
66	13,39,41	Others	4/1	Change 0 ohm to R-Short	0_0402 to R-Short: R2631, R2634, RC168, RC186	PVT	0.3
67	37	Others	4/1	SMT require delete un-use 0 ohm to avoid USB chock solder issue	Del R458, R461, R465, R466	PVT	0.3
68	38	LID	4/1	For 2nd source hall sensor soultion	Mount R618	PVT	0.3
69	30,31	Others	4/1	PD for HPD signal	Add R380 PD100K, Mount R2530	PVT	0.3
70	38	Others	4/1	Board ID Change for PVT	change R4903 to 15K	PVT	0.3
71	42	Others	4/8	Add discharge circuit for +1.05VSDGPU	Mount Q2008, R574, R1001	PVT	0.3
72	30,37,40	Others	4/14	Change 0 ohm to R-Short	0_0402 to R-Short: R368,R369, R370, R371, R372,R373, R374, R375 R473, R474, R475, R476, R477, R478, R479, R480 0_0603 to R-Short: R2135, R2151	PVT	0.3
73	37,38	Others	4/16	Change U77 pin4 control by EC GPIO	link U77.4 to U4901.119 Un-mount R857	PVT	0.3
74	12	CPU	4/17	Follow MOW10, USB2_ID/USB2_VBUSSENSE connect to GND	Change RC130, RC131 to 0 ohm	PVT	0.3
75	40	Audio	4/17	Beep Sound Path from EC	Change R2138, R2140 to 22K and mount R2138	PVT	0.3
76	06	CPU	4/22	Add test point for CATERR#	Add T166	PVT	0.3
77	06	Others	4/22	Cancel JAPS1 Mask to avoide soldering issue	change JAPS1 footprint to ACES_50506-01841-P01_18P-NPM	PVT	0.3
78	22, 25	GPU	4/30	Add Samsung E-Die VRAM Information	Add X76629BOL13/X76629BOL14	PVT	0.3
79	03, 07	CPU	4/30	Add QS sample CPU for BOM Selection	Add UC1 with QJFC@/QJ8N@/QJ8L@	PVT	0.3

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
80	42	Others	5/14	BOM Error	Change R574, R1001, Q2008 to VGA@	Pre-MP	1.0
81	38	Others	5/28	For abnormal shutdown	Mount D26	Pre-MP	1.0
82	38	Others	5/28	Board ID change to Rev1.0	Change R4903 to 20K_0402_1%	Pre-MP	1.0
83	01	Others	6/17	Update PCB Rev10 PN	Update PCB PN to DAZ1DR00100	Pre-MP	1.0
84	39	Others	6/22	Cancel the MASK of JLID1	Change JLID1 to ACES_50506-01041-P01_10P-NPM	Pre-MP	1.0
85	38	Others	7/14	Add C4917 for EC_RST#	Add C4917	Pre-MP	1.0
86	39	Others	7/14	Add S spec number for i3/i5/i7 CPU	add SR2EU@/SR2EY@/SR2EZ@ for UC1 MP number	Pre-MP	1.0